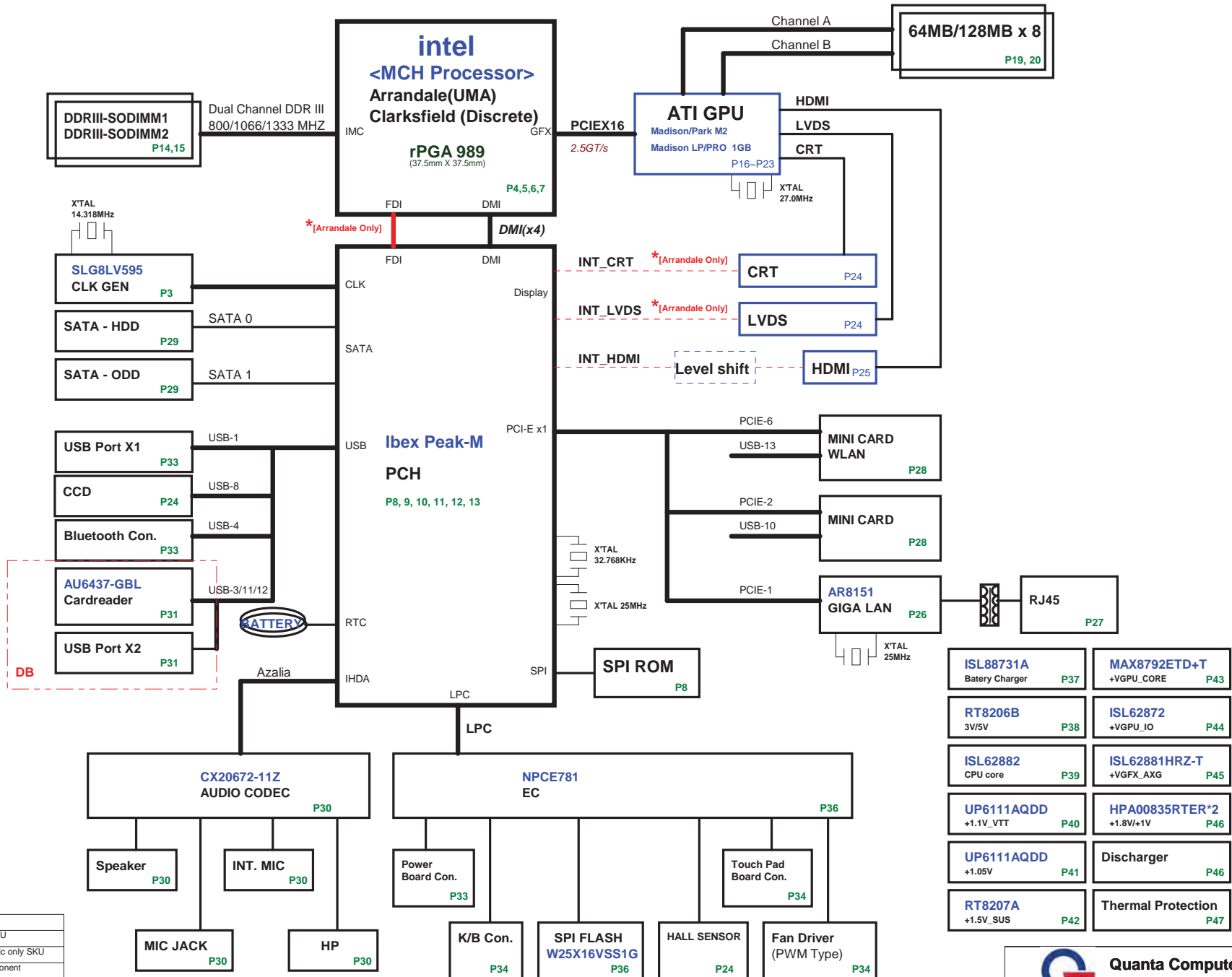
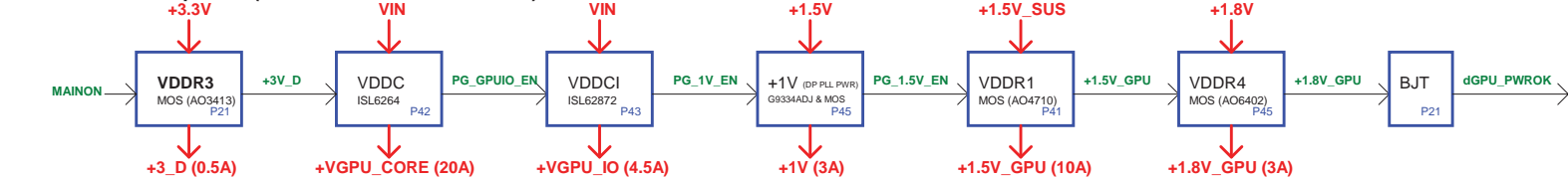


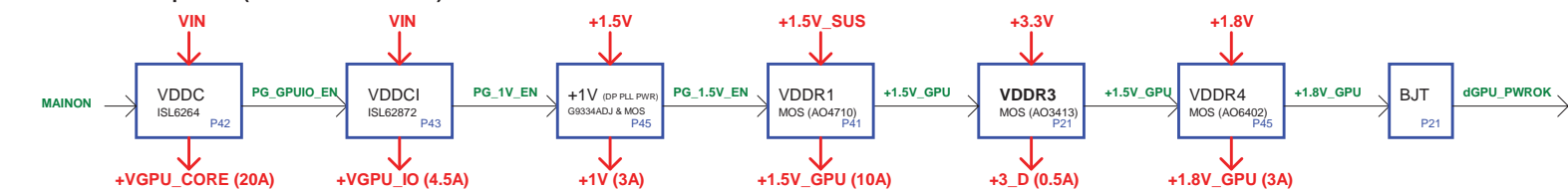
ZYD SYSTEM BLOCK DIAGRAM



GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



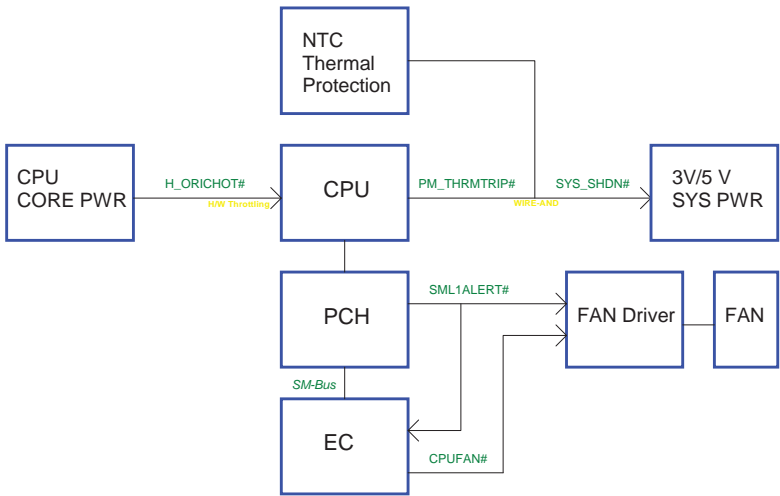
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



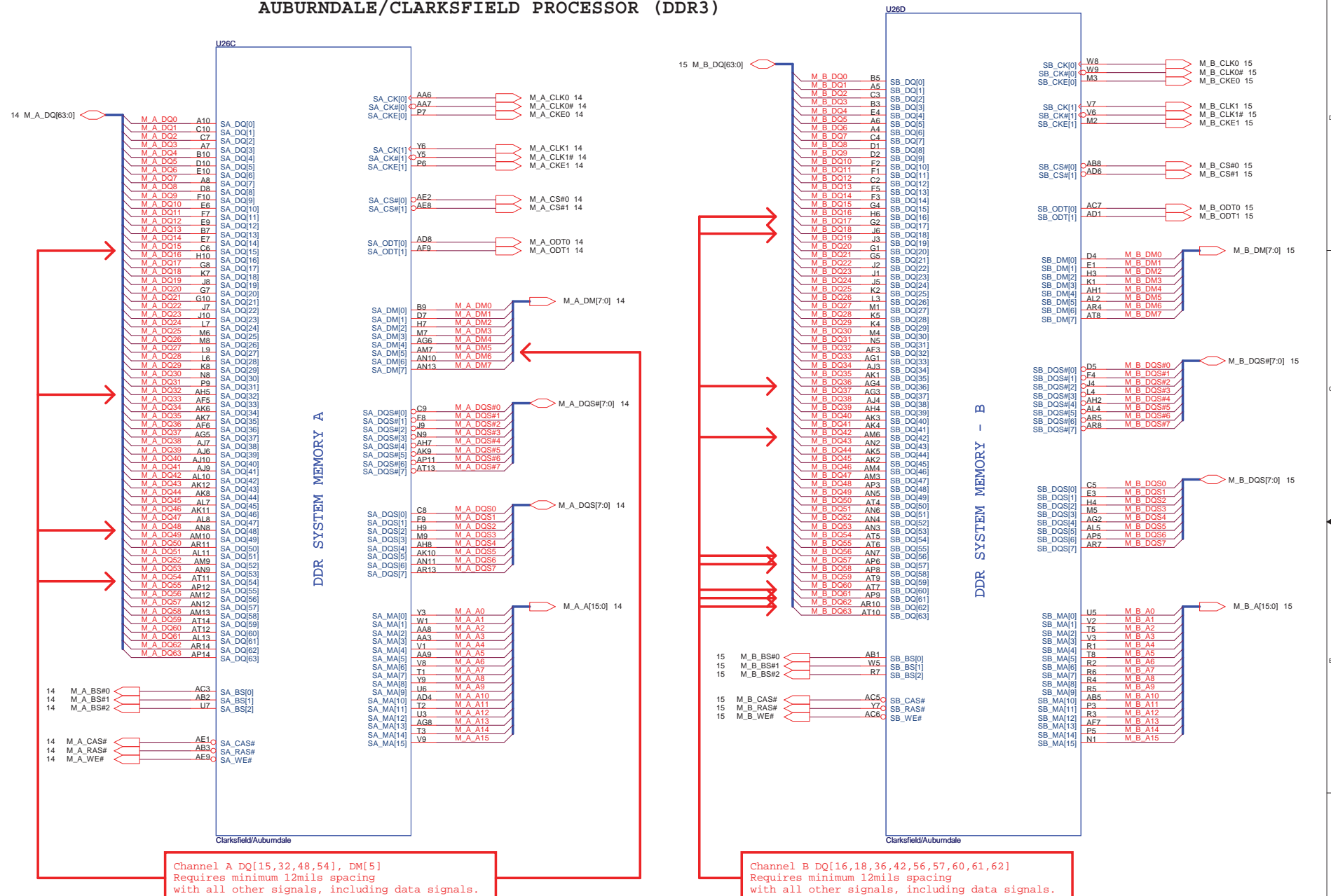
Power States

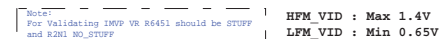
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/PCH	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT	MAINON	S0
+3V	+3.3V	CLK GEN/PCH/GPU/LVDS/Mini card/Codec/card MAINON	MAINON	S0
+1.5V_SUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+3V_D	+3.3V	I/O POWER for 3.3V pins	dGPU_VRON	Discrete enable
+VGPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+VGPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable

Thermal Follow Chart




AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



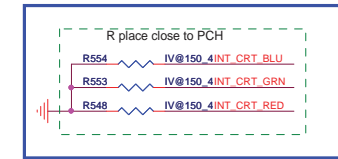
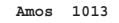


AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)

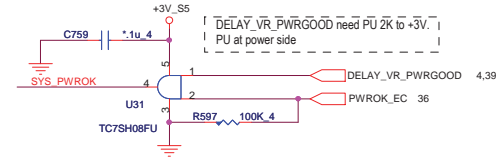


 Quanta Computer Inc. PROJECT : ZYD		Rev 3B
Size	Document Number AUBURND 4/4	
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IBEX PEAK-M (LVDS, DDI)

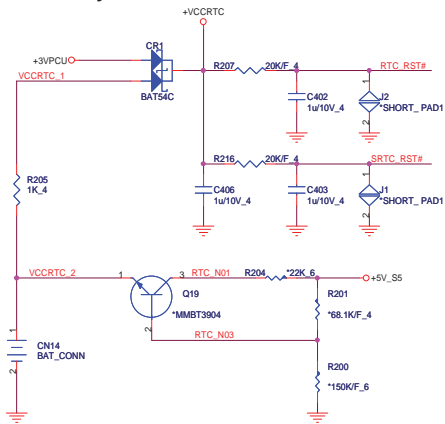


System PWR_OK



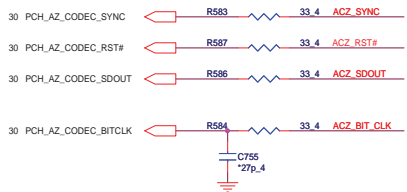
WWW.AliSaler.Com

RTC Circuitry

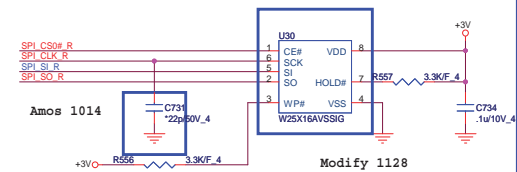


HDA_SYNC (PCH strap pin)
Internal weak pull-down
VCCVRM=>+1.5V (default)
external pull-up
VCCVRM=>+1.5V

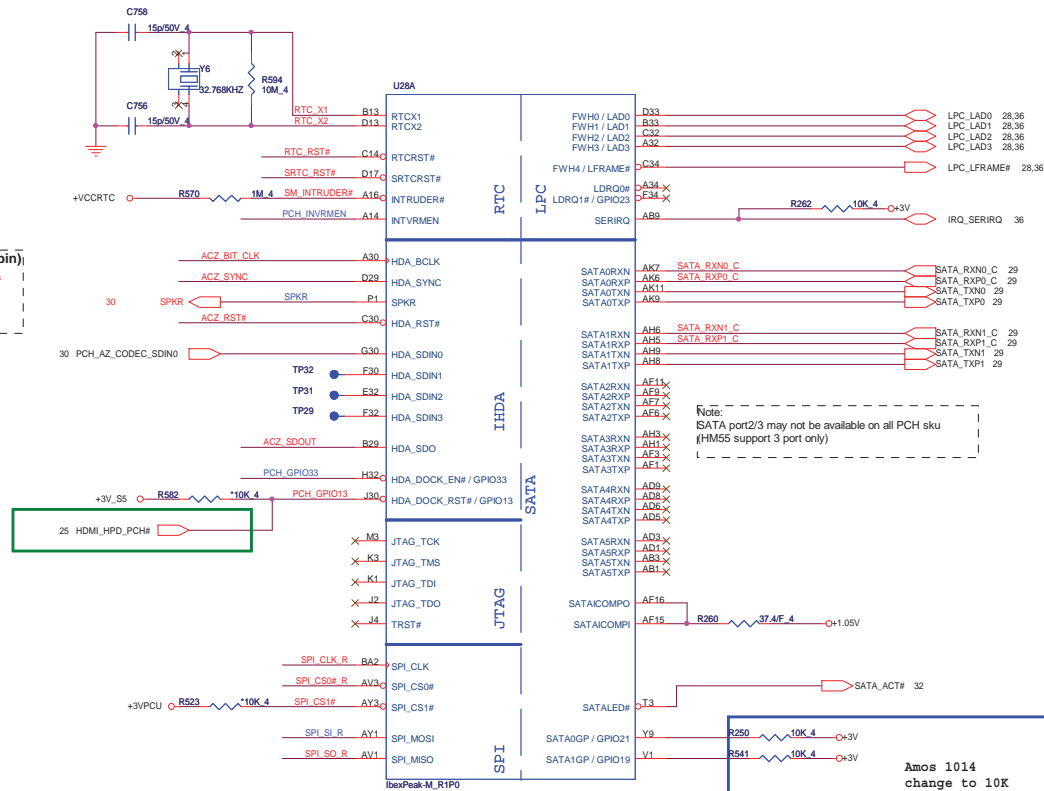
HDA Bus



MDC Bus



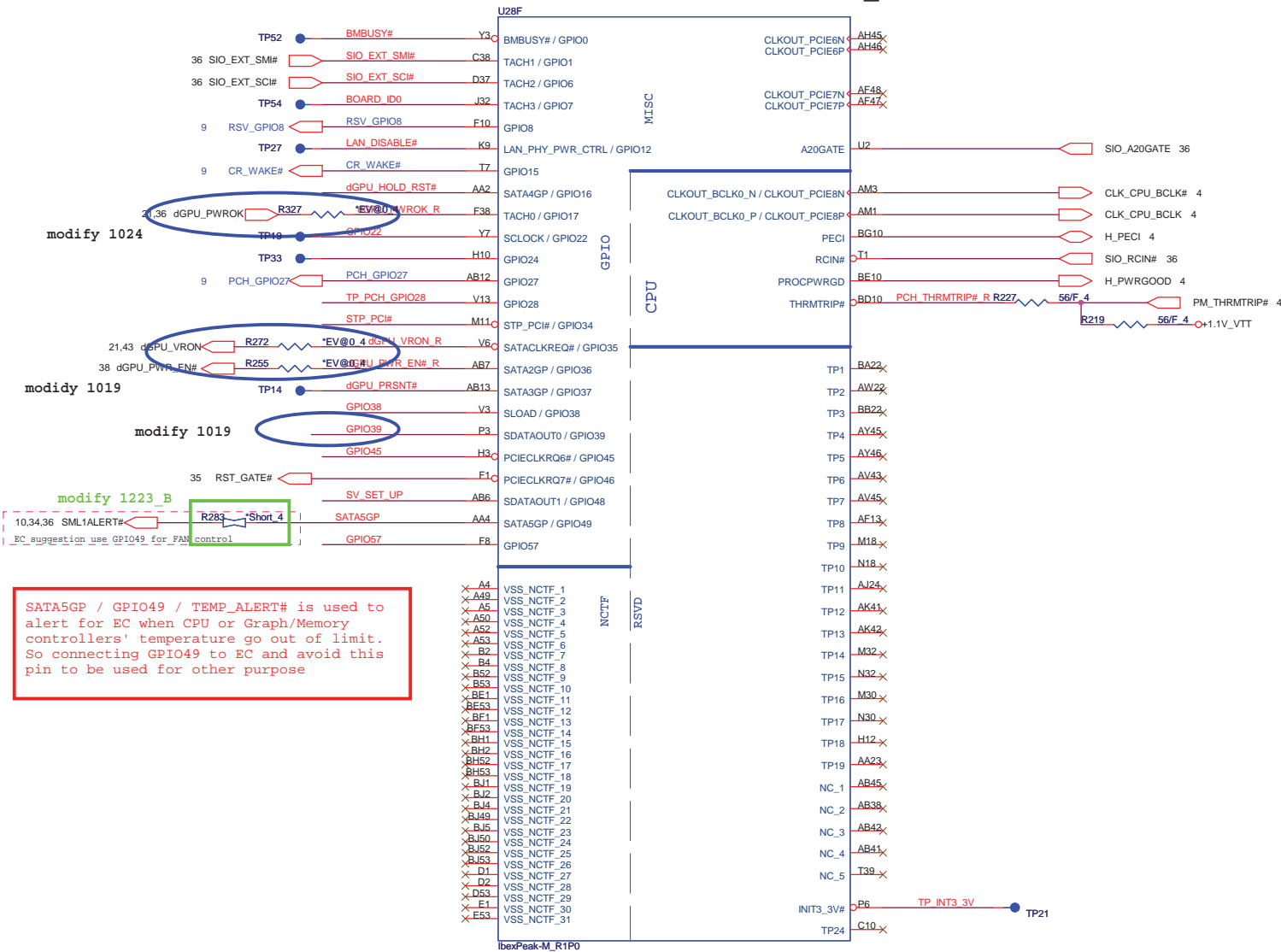
PCH SPI



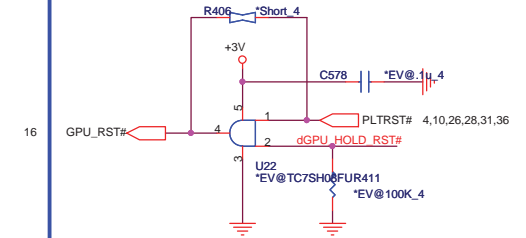
PCH Strap Pin Configuration Table-1

INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC R593 330K 6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V R559 1K 4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V R307 1K 4 SPKR
HDA_DOCK#EN #/GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 J3 1 2 R322 10K 4
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	10 PCI_GNT0# R315 1K 4 10 PCI_GNT1# R310 1K 4
GNT2#/GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	10 PCI_GNT2# R313 1K 4
GNT3#/GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	10 PCI_GNT3# R560 10K 4
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	10 NV_ALE R231 1K 4 +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	10 NV_CLE R230 1K 4 +1.8V
GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	8SV_GPIO8 R325 10K 4 +3V_SS R320 1K 4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	CR_WAKE# R282 1K 4 +3V_SS
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	11 PCH_GPIO27 R263 10K 4

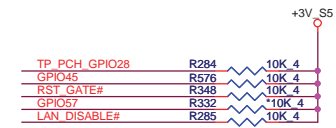
IBEX PEAK-M (GPIO, VSS_NCTF, RSVD)



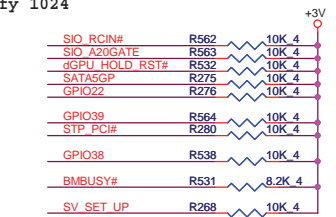
GPU RST#



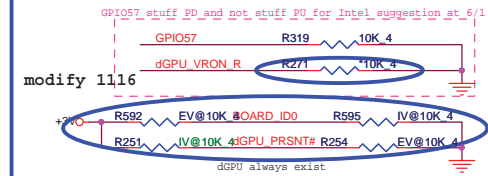
GPIO Pull-up/Pull-down



modify 1024



SV_SET_UP	1-X High = Strong (Default)
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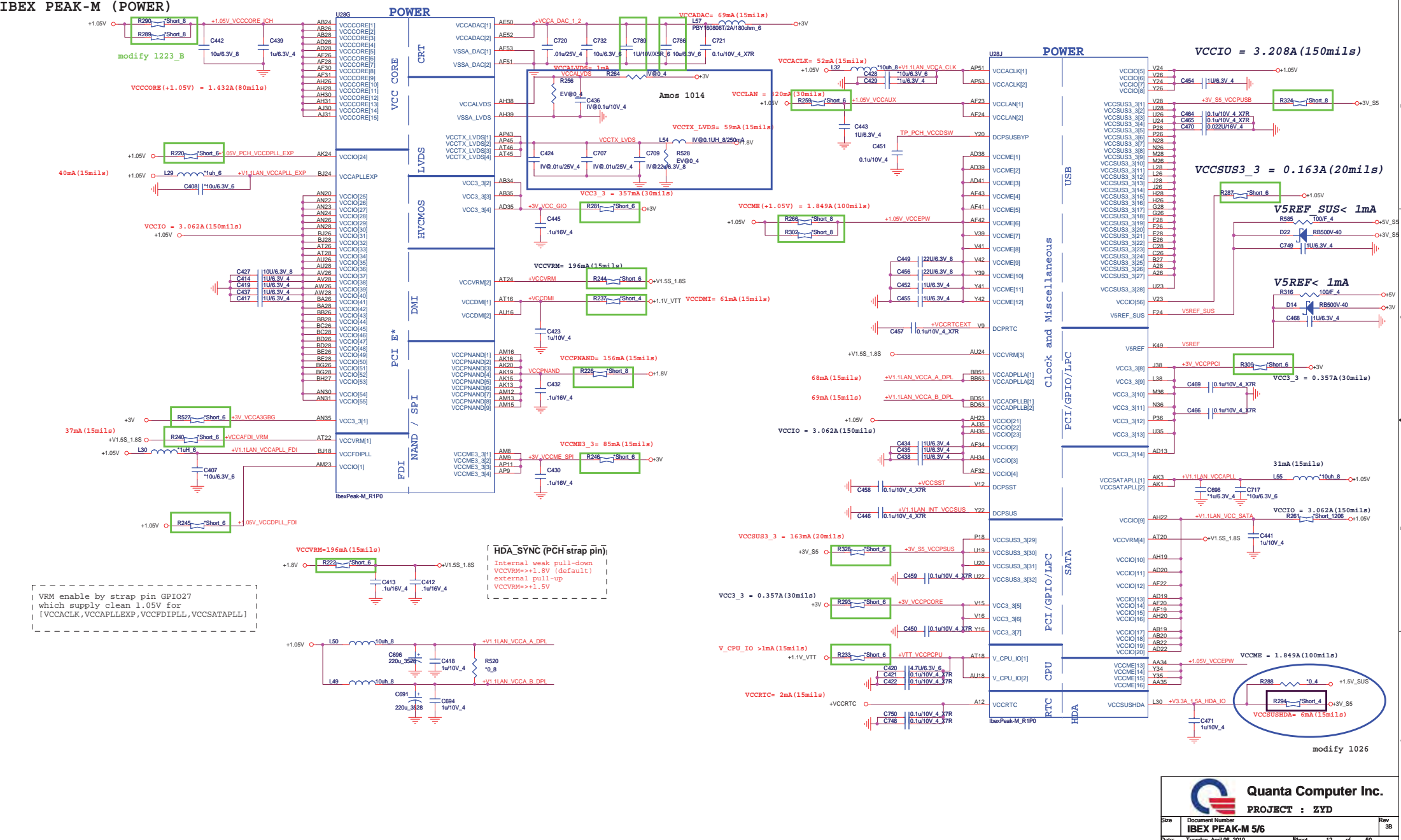
modify 1116

Integrated Clock Chip Enable	
BOARD_ID0	High = Discrete Low = IV
RSV_GPIO8	High = Disable Low = Enable

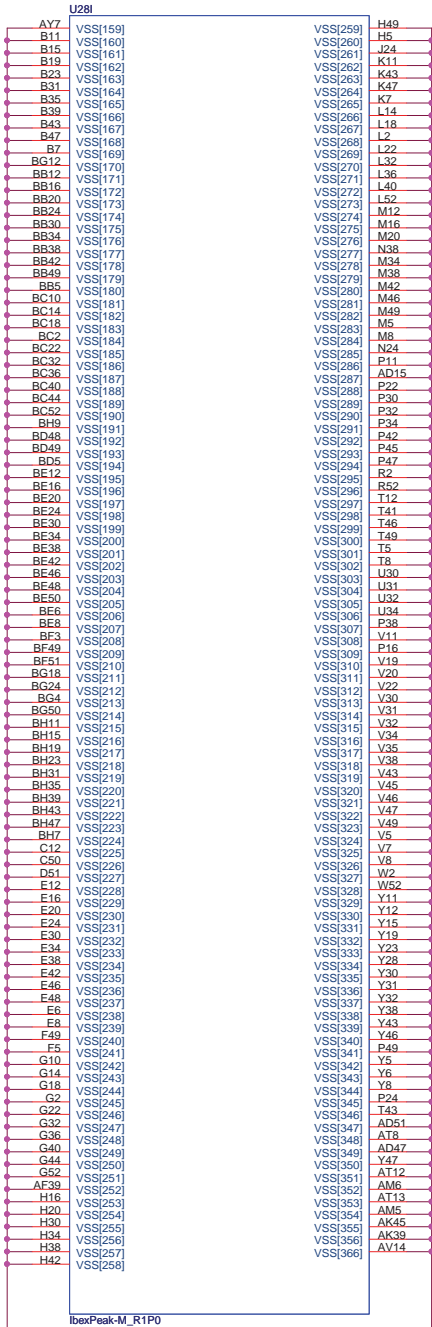
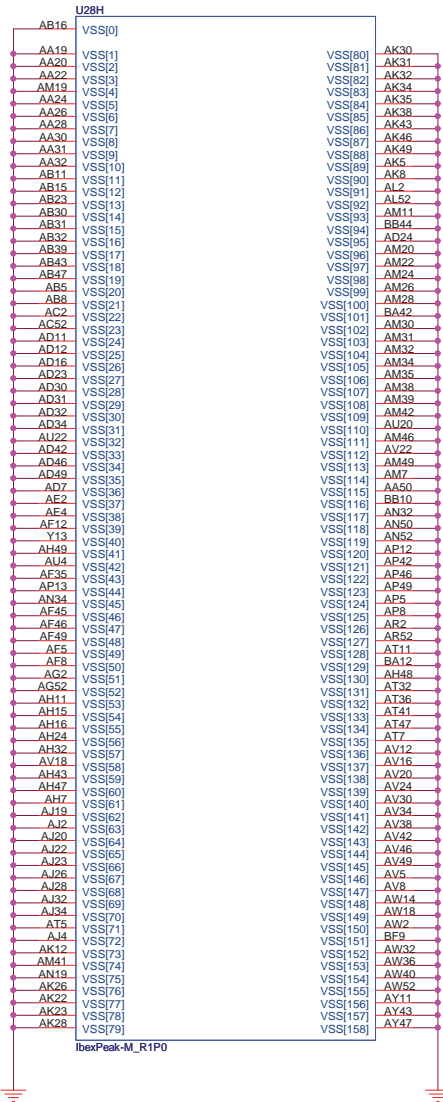


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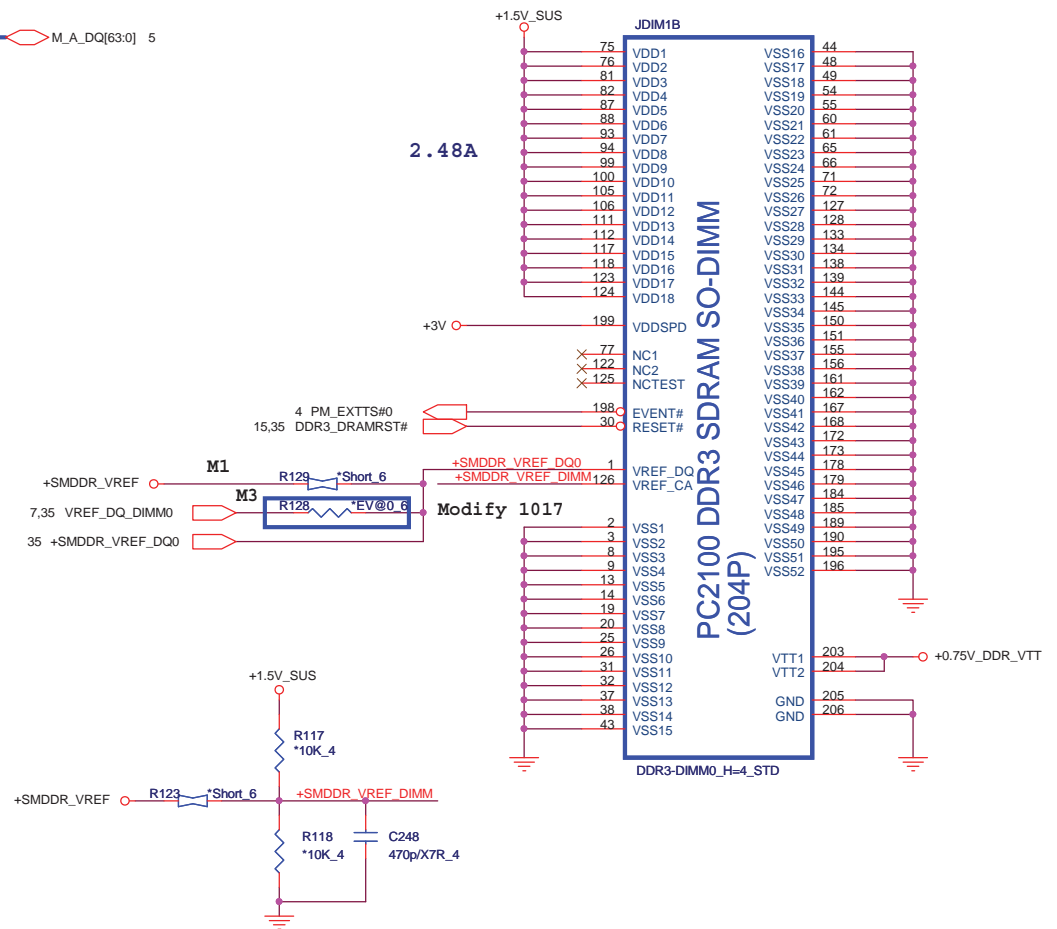
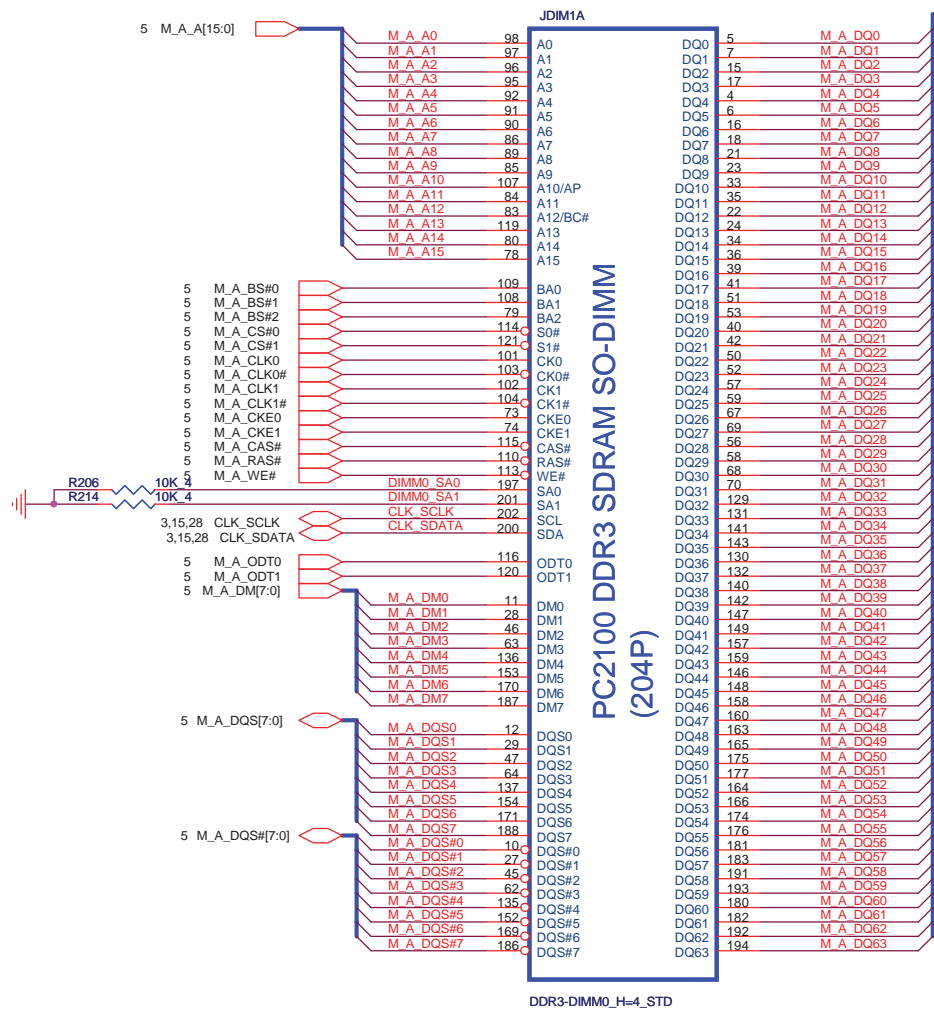
IBEX PEAK-M (POWER)



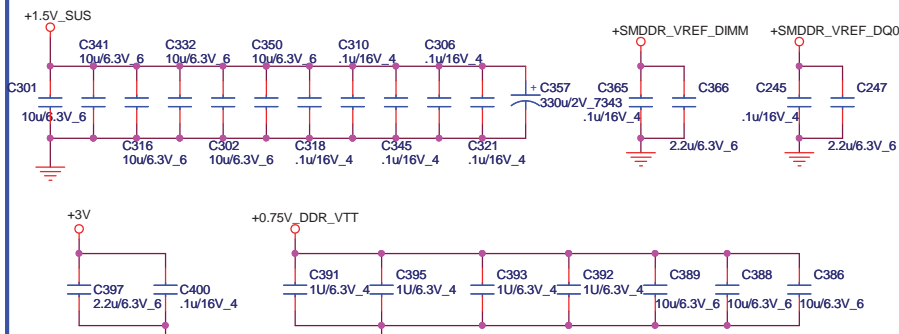
IBEX PEAK-M (GND)



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Place these Caps near So-Dimm0.

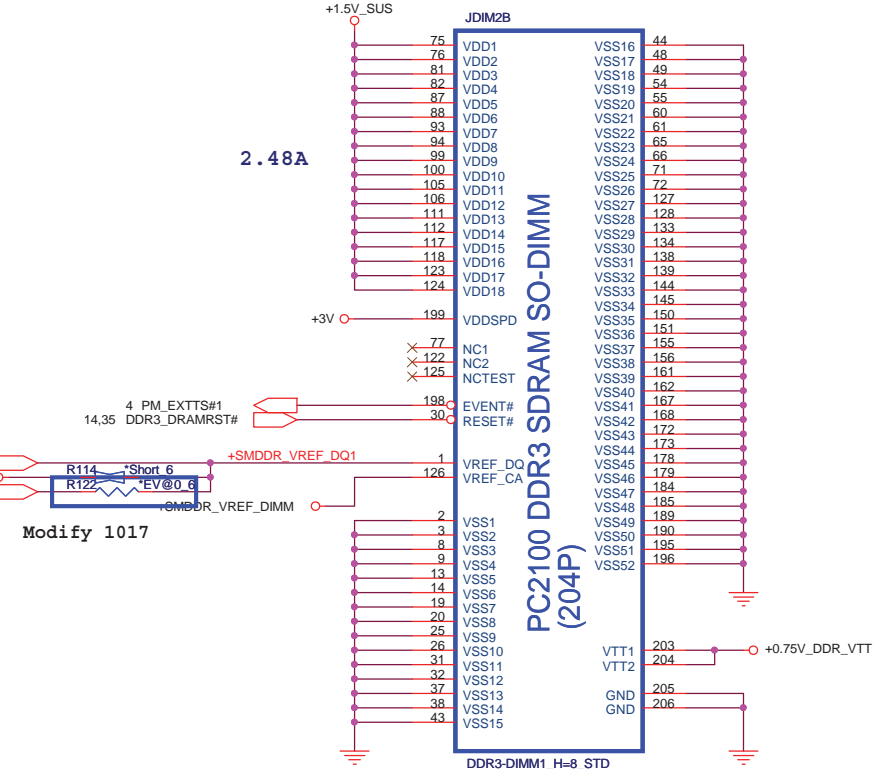
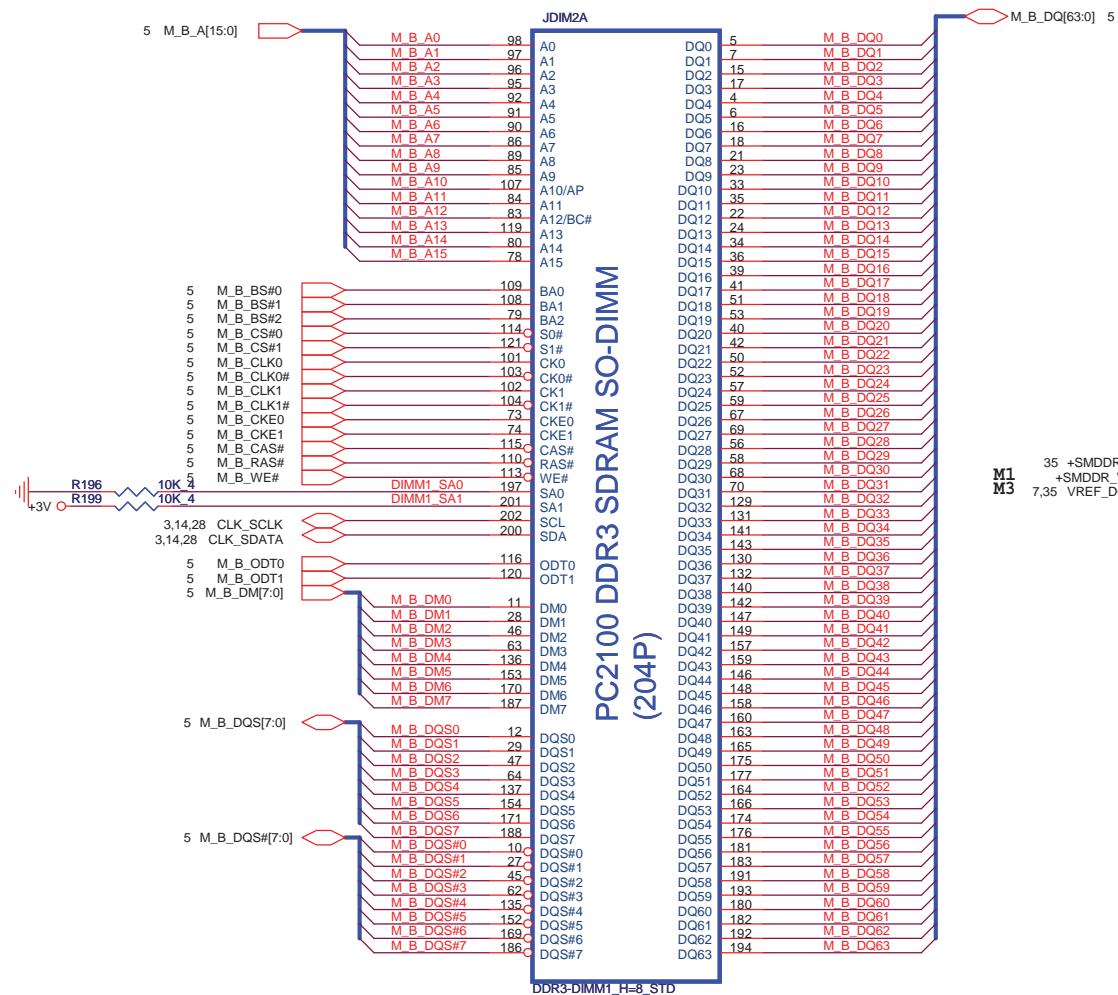


For Arrandale only designs--->Only method M1 should be enabled.
For Clarkfield only designs--->Both M1 AND M3 methods should be enabled simultaneously.
For Common Motherboard designs--->Both M1 AND M3 methods should be enabled simultaneously.

M1:PWR SMDRR_VREF
M1+:voltage divider(Default)
M3:CPU VREF_DQ_DIMM0

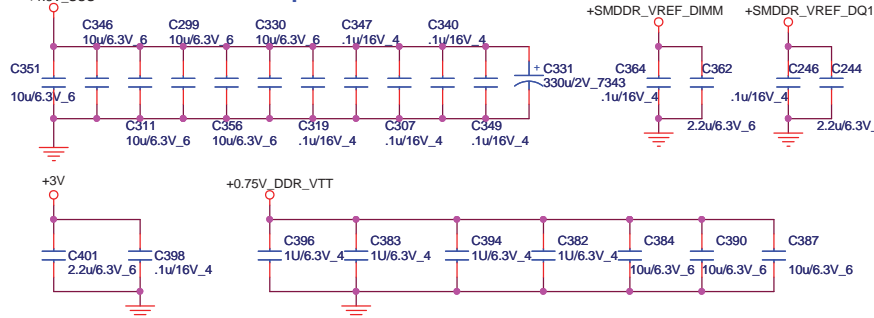


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Modify 1017

Place these Caps near So-Dimm1.

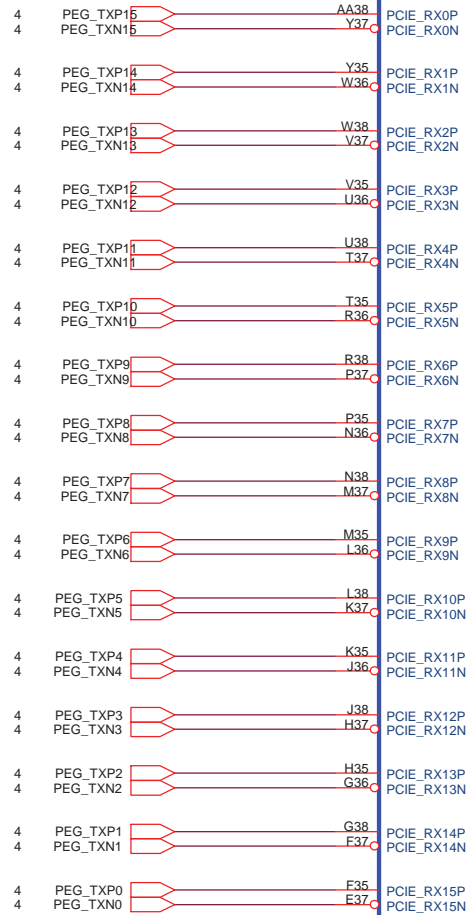


For Arrandale only designs--->Only method M1 should be enabled.
For Clarksfield only designs--->Both M1 AND M3 methods should be enabled simultaneously
For Common Motherboard designs--->Both M1 AND M3 methods should be enabled simultaneously.



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U18A



CLOCK
PCIE_REFCLKP
PCIE_REFCLKN

EV@Madison/Park_M2

PCI EXPRESS INTERFACE

CALIBRATION



+1.0V

For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V



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PROJECT : ZYD

Size	Document Number	Rev
	Madison/Park M2 PCIE I/F	3B
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GPU Power-on sequence

- 1 => +VGPU_CORE
- 2 => +VGPU_IO
- 3 => +1V
- 4 => +1.5V_GPU
- 5 => +3V_D
- 6 => +1.8V_GPU
- 7 => dGPU_PWROK

1.8V GPIO

NC on Park

NC on Park

+3V_D

R50

EV@10K_F_4

R56

EV@10K_F_4

R58

EV@10K_F_4

R59

EV@10K_F_4

R60

EV@10K_F_4

R61

EV@10K_F_4

R62

EV@10K_F_4

R63

EV@10K_F_4

R64

EV@10K_F_4

R65

EV@10K_F_4

R66

EV@10K_F_4

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EV@10K_F_4

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R80

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R105

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R107

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R108

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R161

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EV@10K_F_4

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R189

EV@10K_F_4

R190

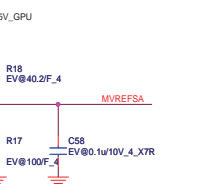
EV@10K_F_4

R191

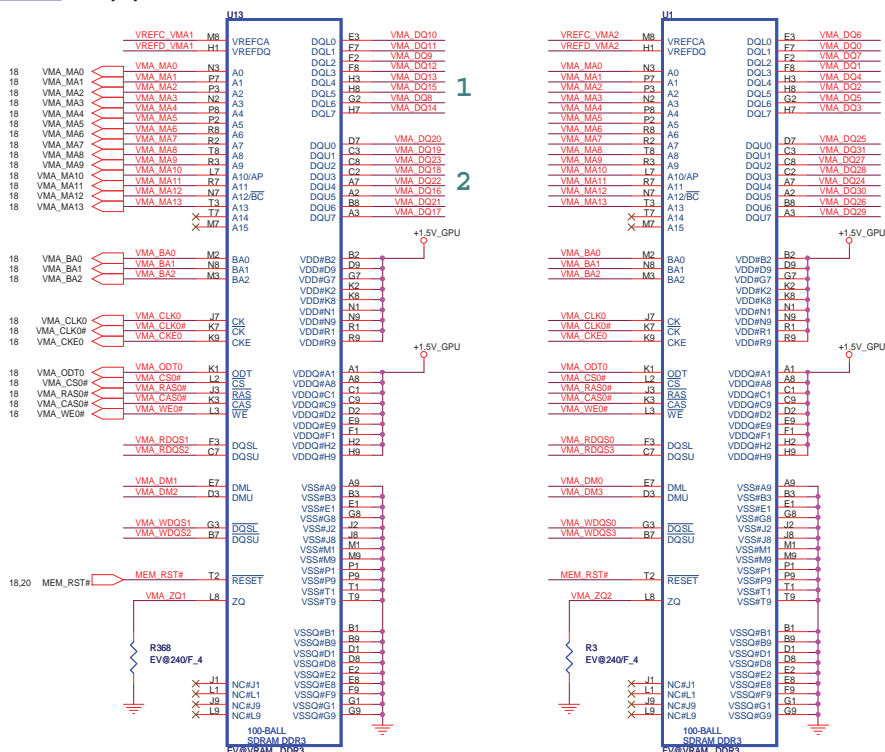
EV@10K_F_4

R192

EV@10K_F_4

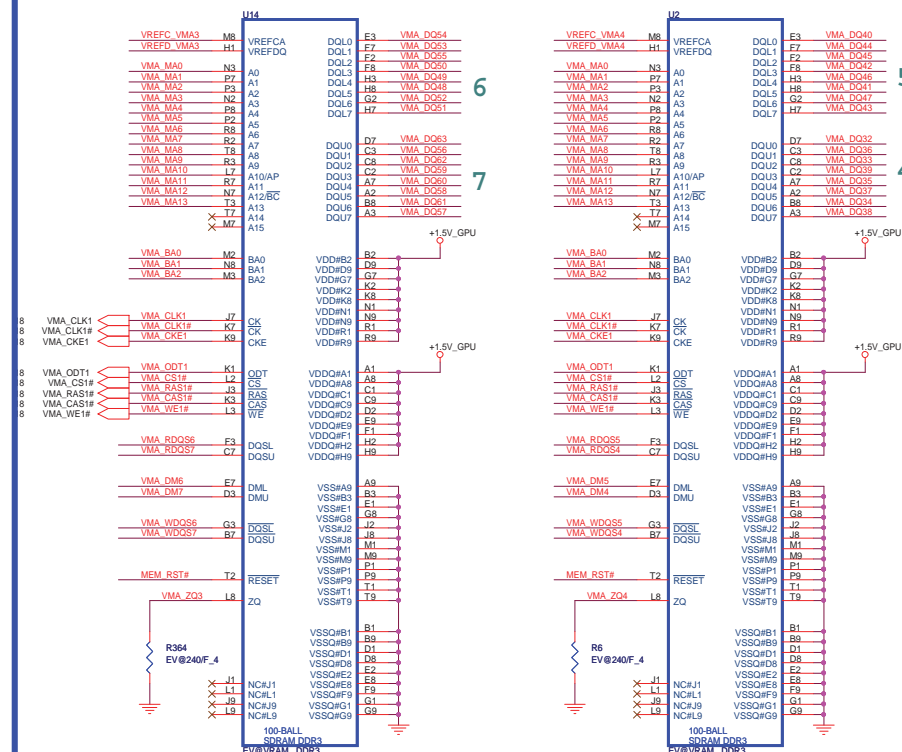


Park, M92M Use Channel B Memory Interface Only



TOP Left

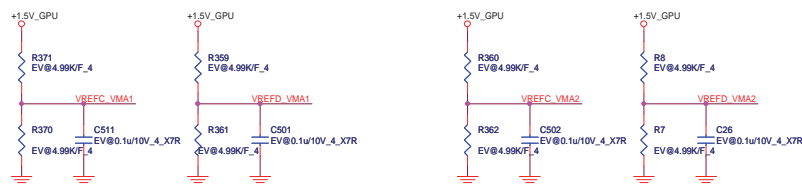
BOT Left



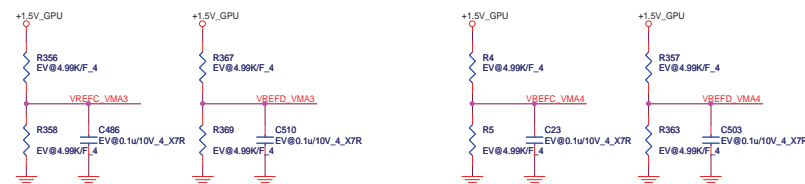
BOT Right

TOP Right

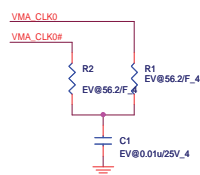
Group-A0 VREF



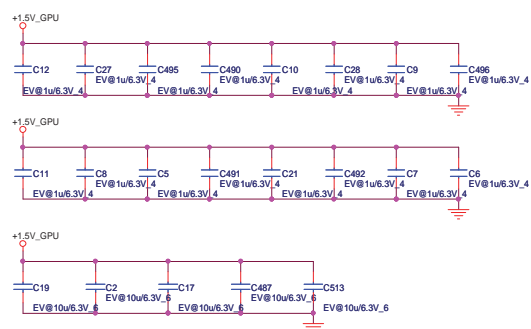
Group-A1 VREF



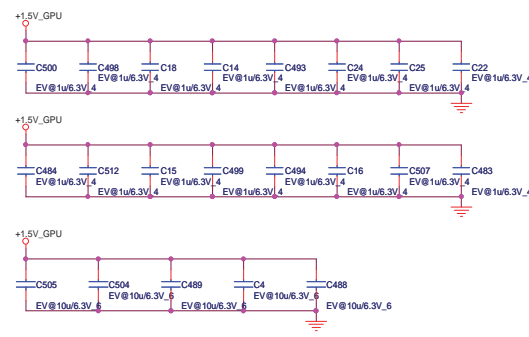
MEM A0 CLK



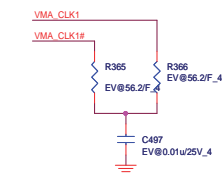
Group-A0 decoupling CAP



Group-A1 decoupling CAF



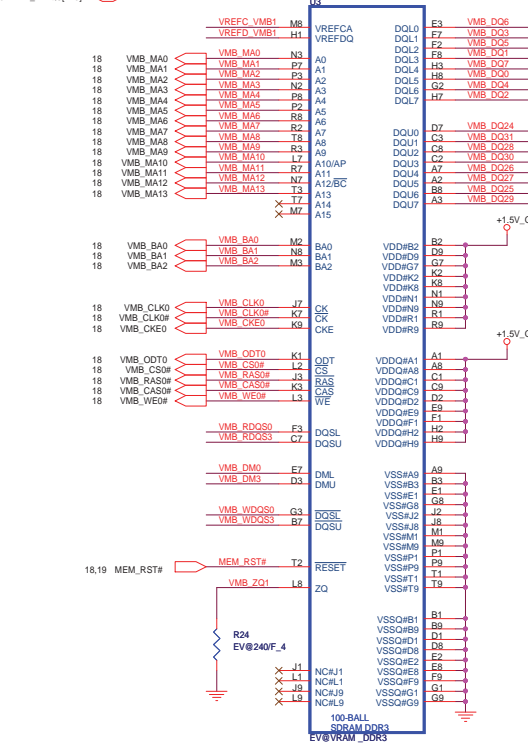
MEM A1 CLK



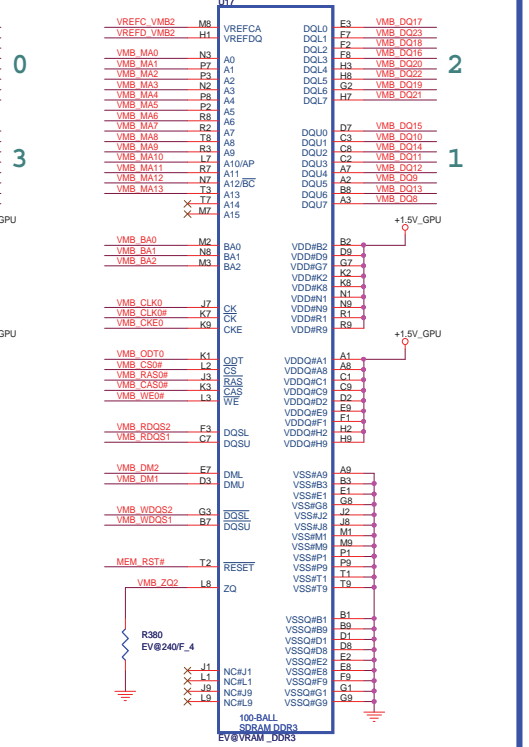
CHANNEL B: 512MB DDR3 (64M*16*4pcs)

18 VMB_DQ[63..0] VMB_DQ[63..0]
18 VMB_DM[7..0] VMB_DM[7..0]
18 VMB_RDOQ[7..0] VMB_RDOQ[7..0]
18 VMB_WDOQ[7..0] VMB_WDOQ[7..0]

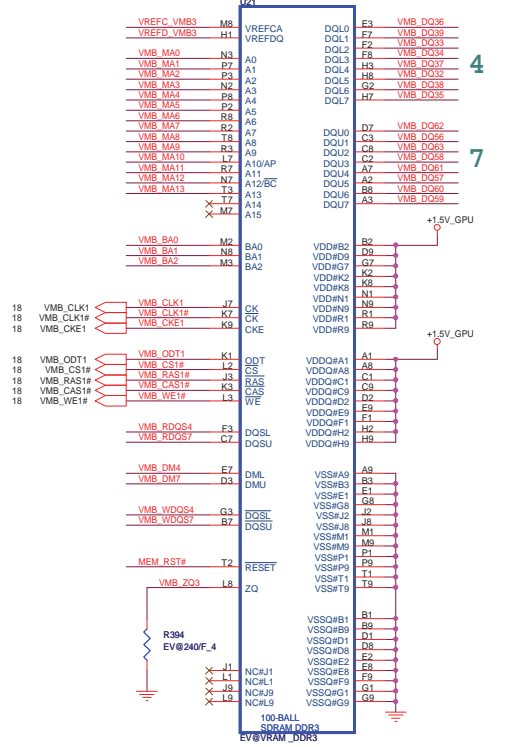
QSA[7..0]
QSA[7..0]



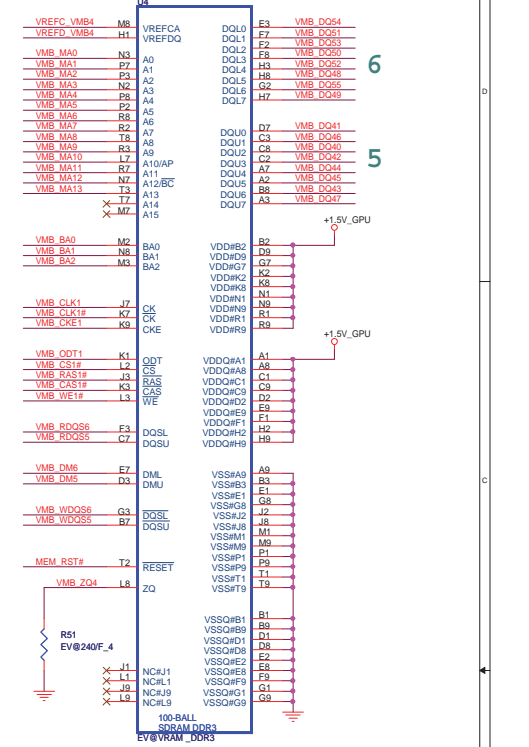
BOT Down



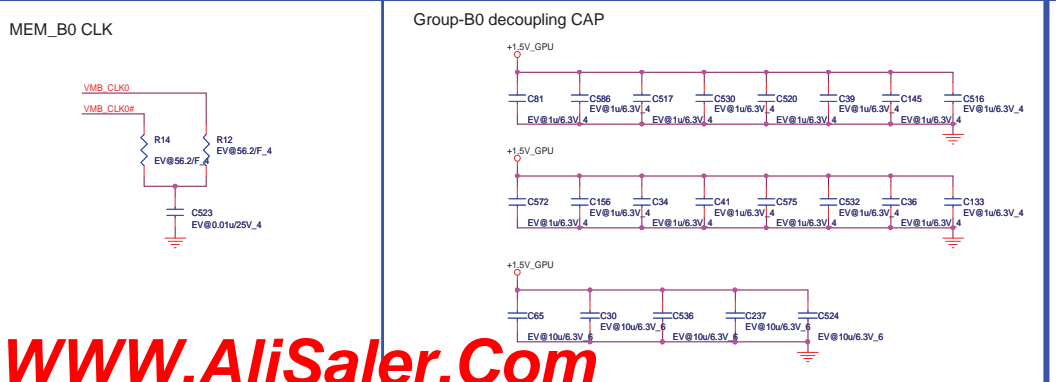
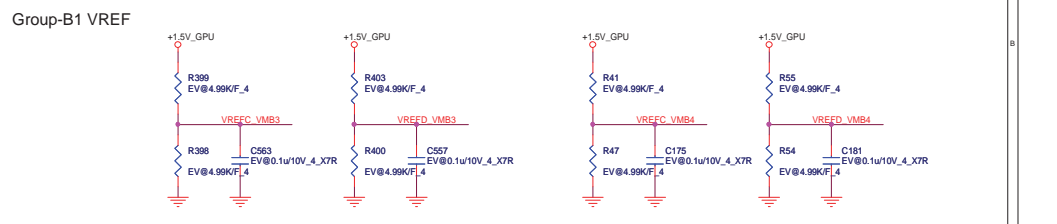
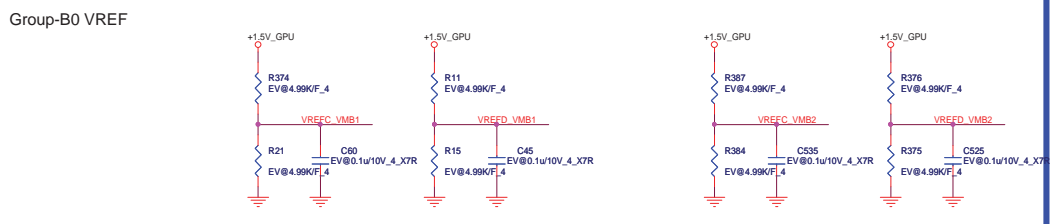
TOP Down



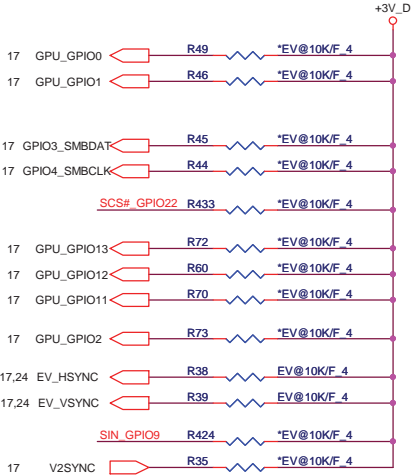
TOP Up



BOT Up



PIN STRAPS



Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

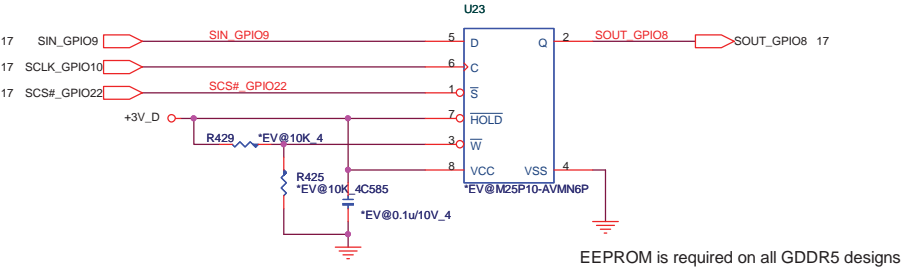
Audio Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

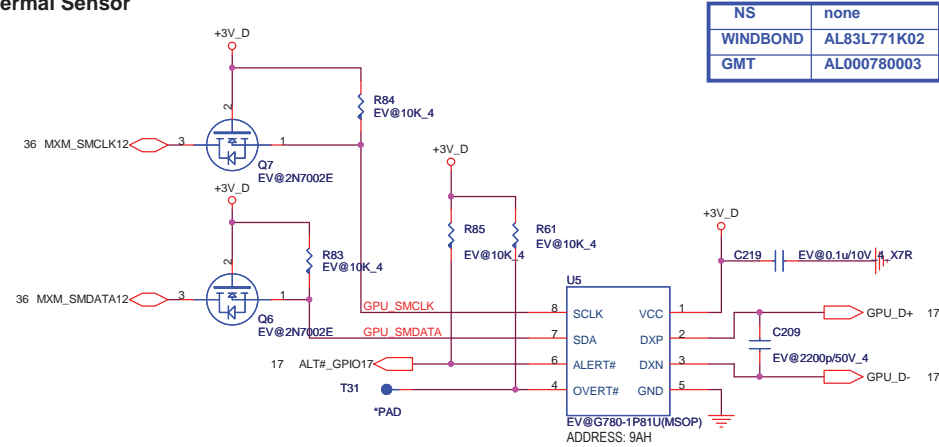
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	000	See Memory Aperture size
BIF_GEN2_EN_A	GPIO2	0 = PCIe DEVICE AS 2.5GT/S CAPABLE 1 = PCIe DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

EEPROM

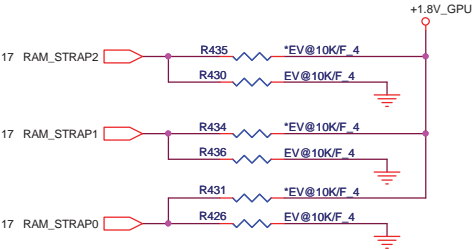


Thermal Sensor



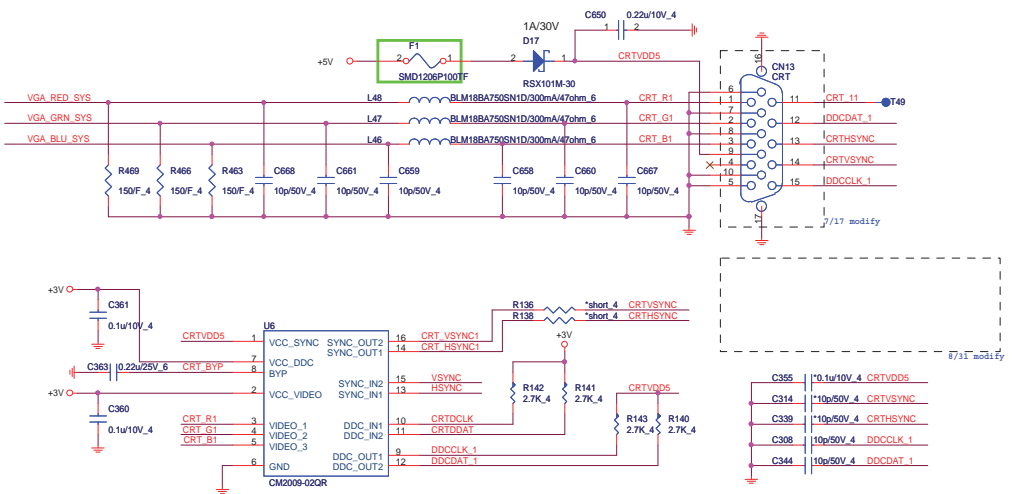
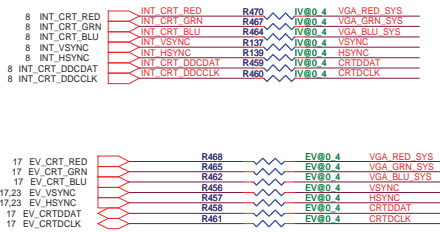
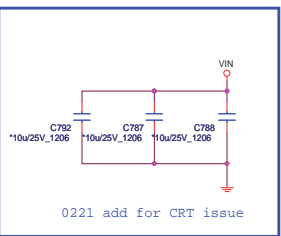
DDR3 Memory Aperture size

DDR3 VRAM size						
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	512MB	1	1	0
			1GB	1	0	0
			2GB	1	0	1
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	512MB	0	1	0
			1GB	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1
AMD	23EY2387MA-12	AKD5LGGT700		0	1	0

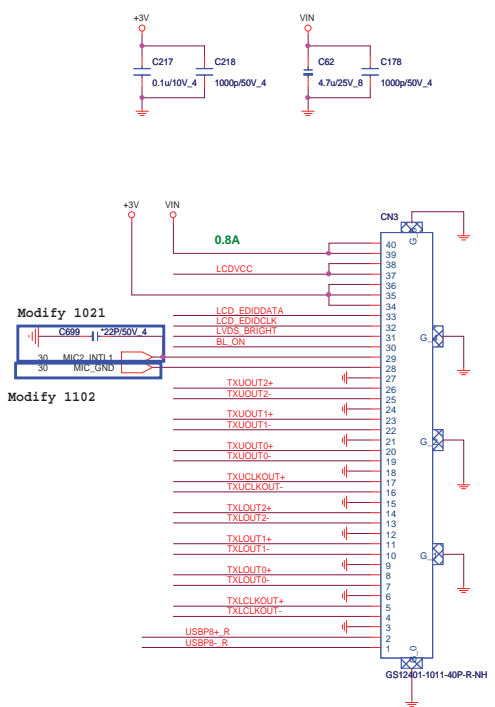
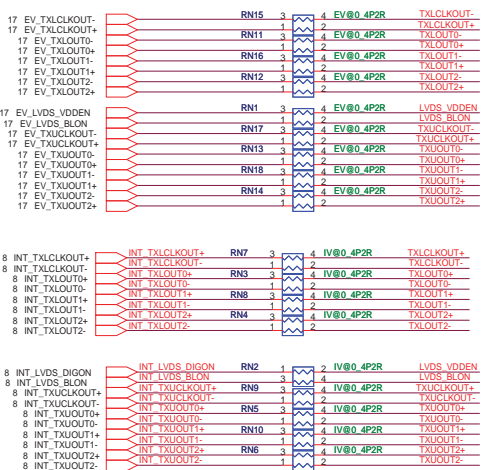
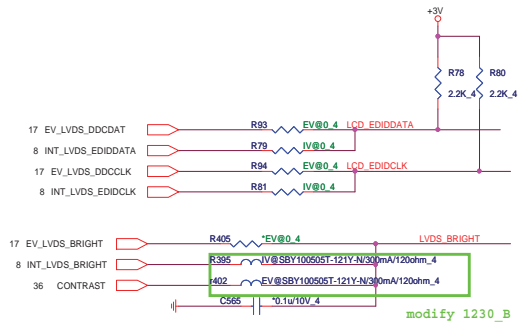


RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

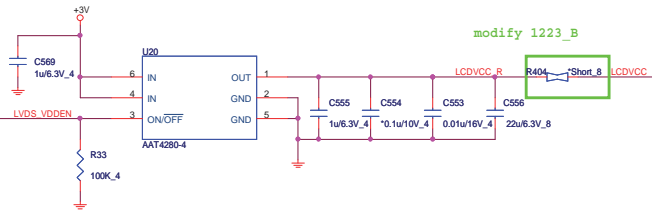
CRT(CRT)



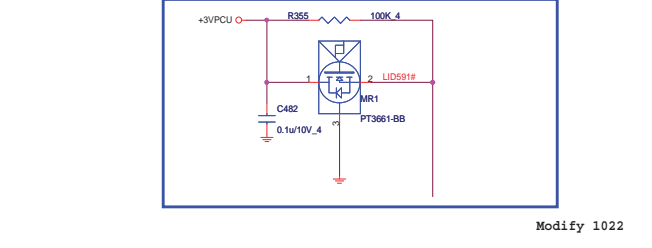
LVDS(LDS)



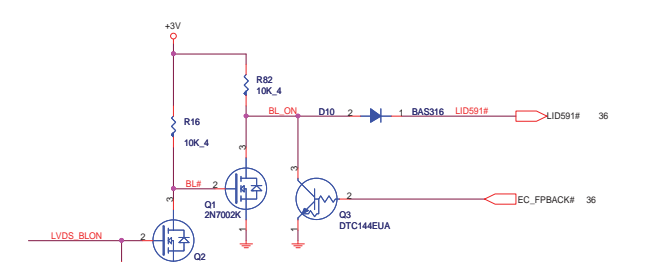
LCD Power(LDS)



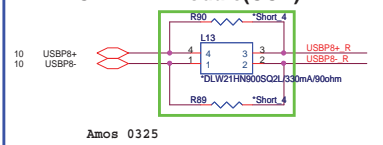
Hall Sensor(HSR)



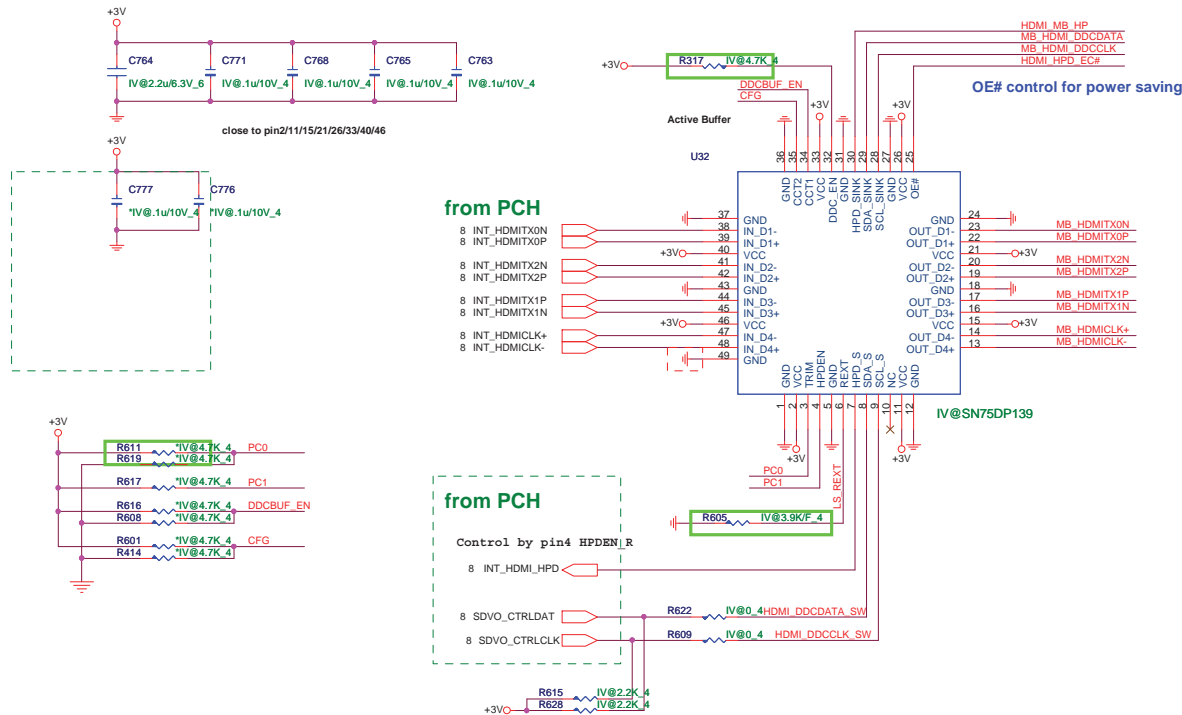
Backlight Control(LDS)



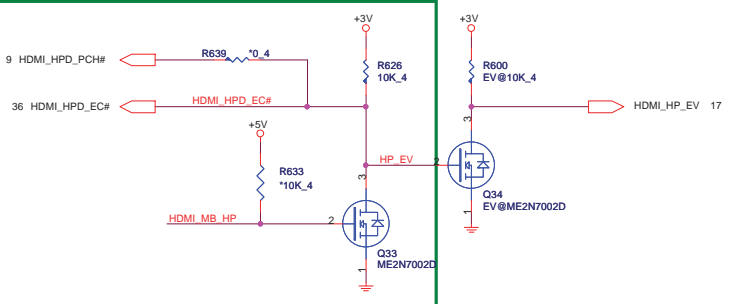
CAMERA Module(CCD)



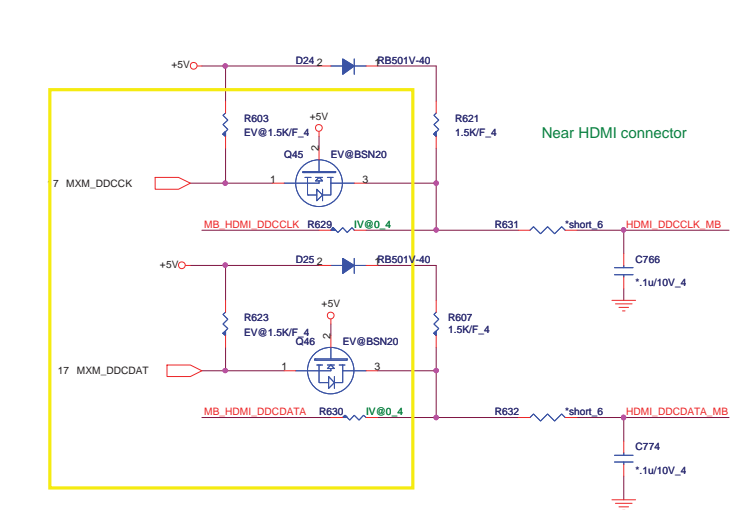
IV @ HDMI LEVEL SHIFTER



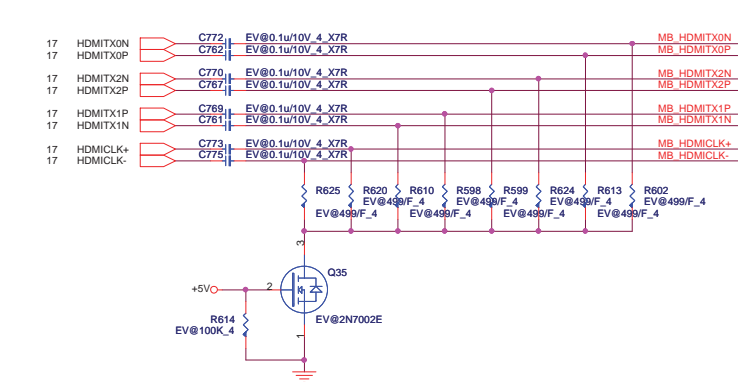
HDMI-detect



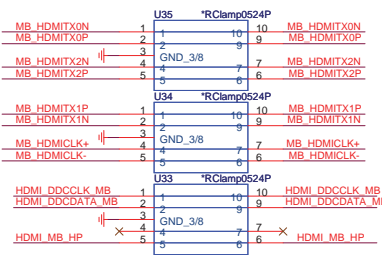
I2C



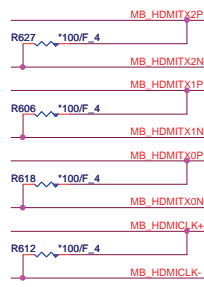
External Graphic HDMI source



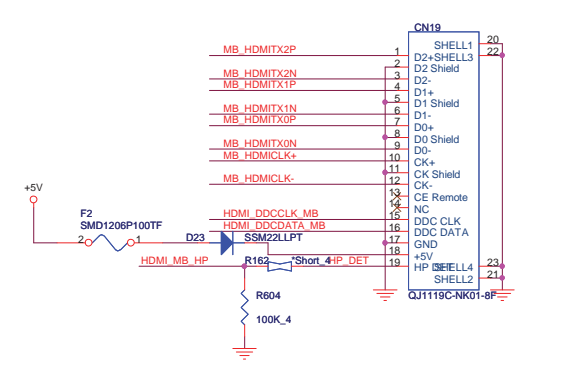
ESD Protect



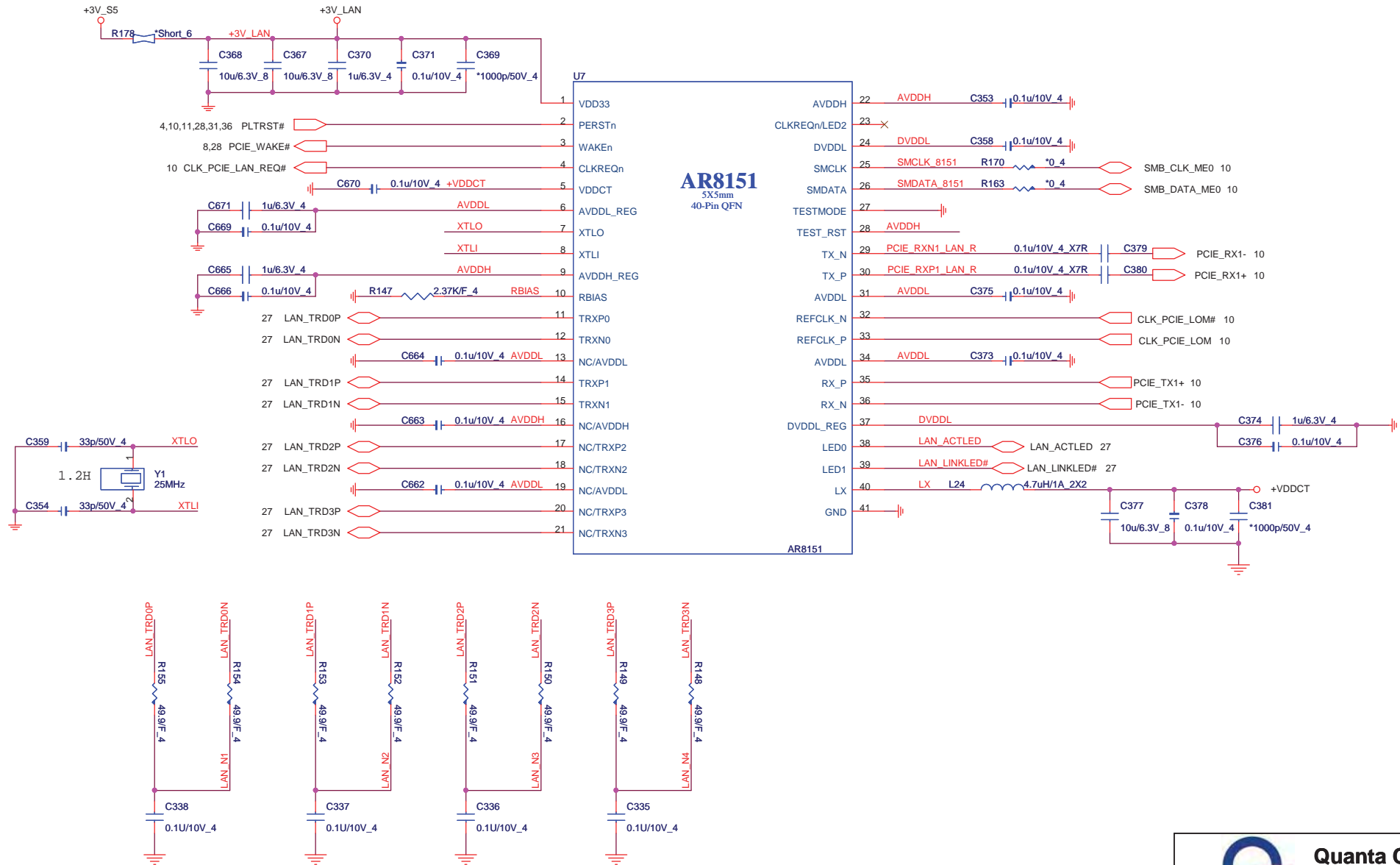
EMI




HDMI connector

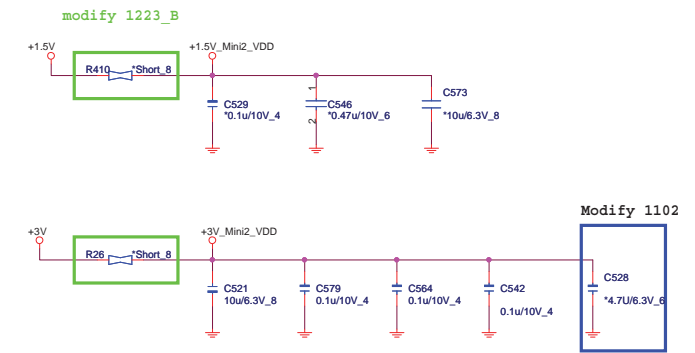


Giga-LAN AR8151

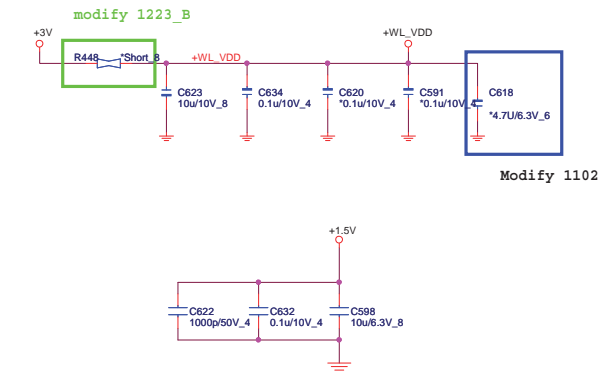


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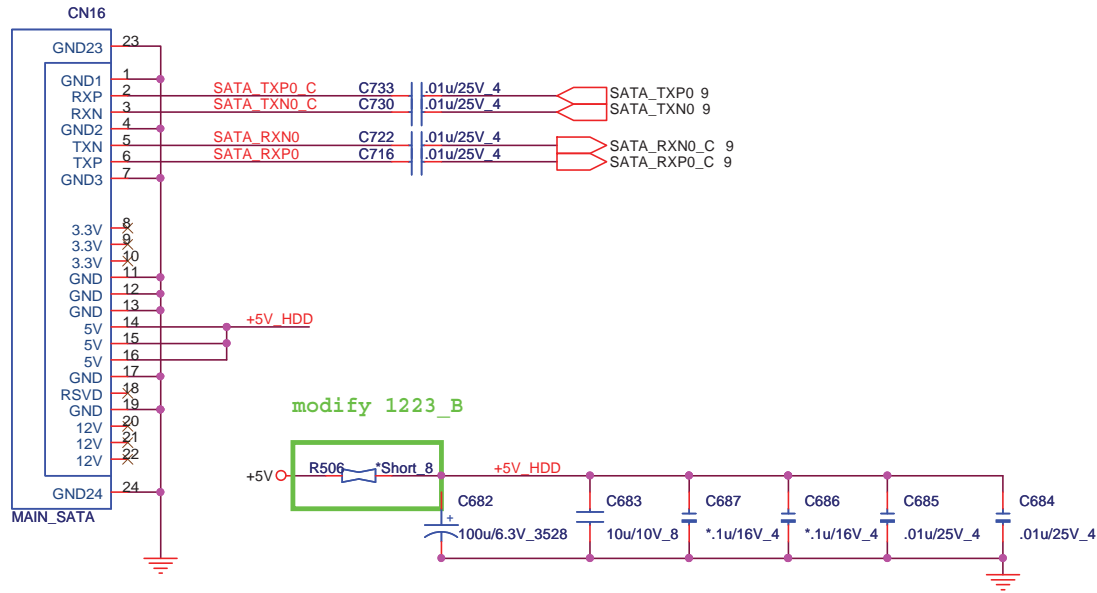
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA



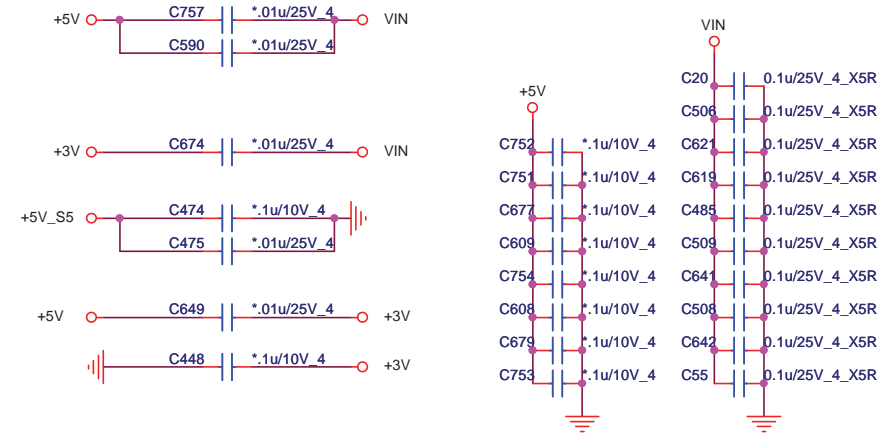
Check LED signal. (active high or low)



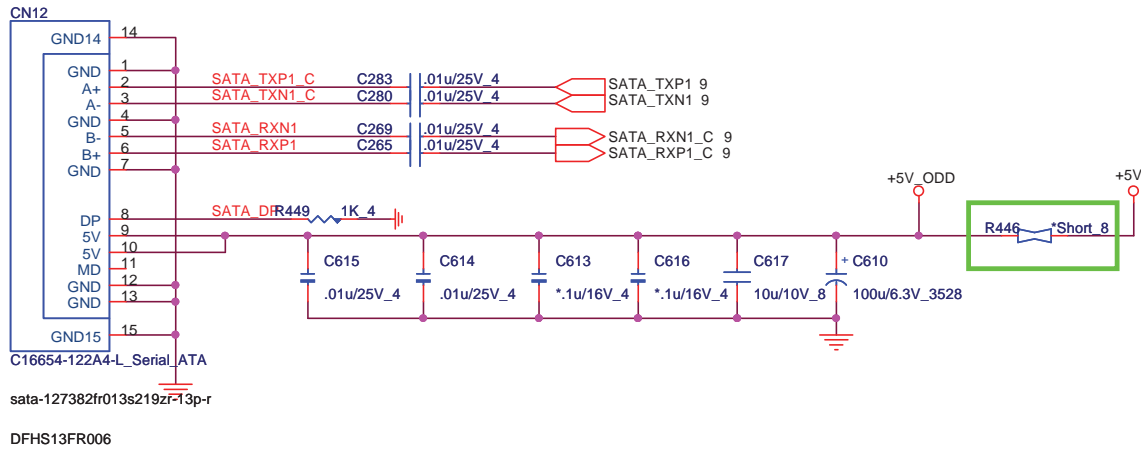
MAIN SATA HDD



EE RETURN-PATH CAPACITORS

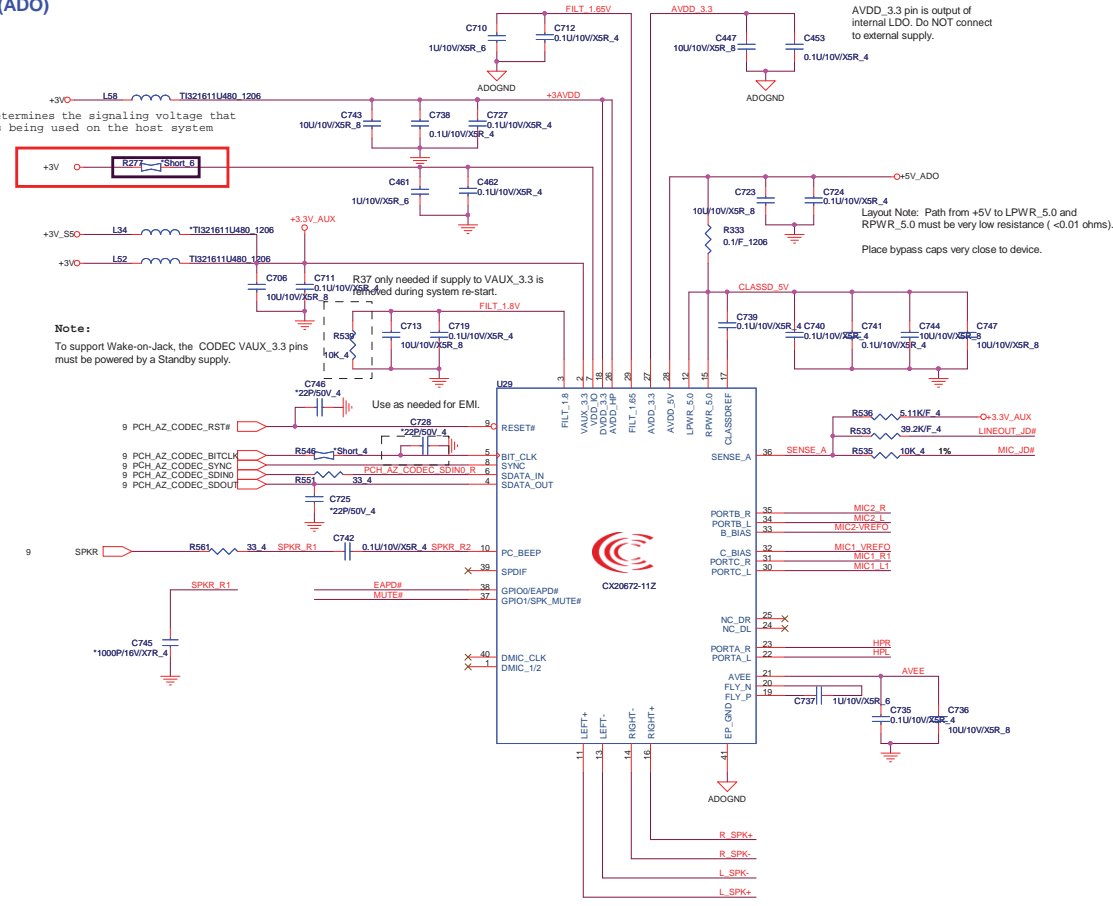


ODD (SATA)

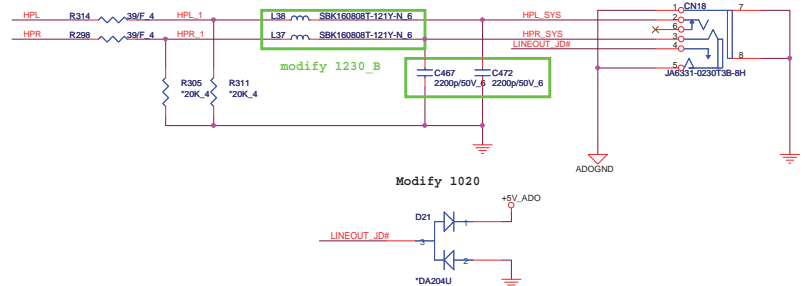


Codec(ADO)

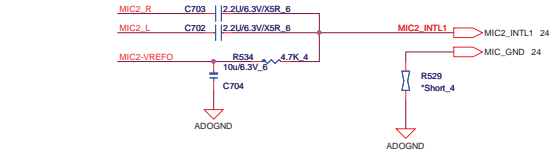
(CX20672-11Z for QFN)
(ADO)



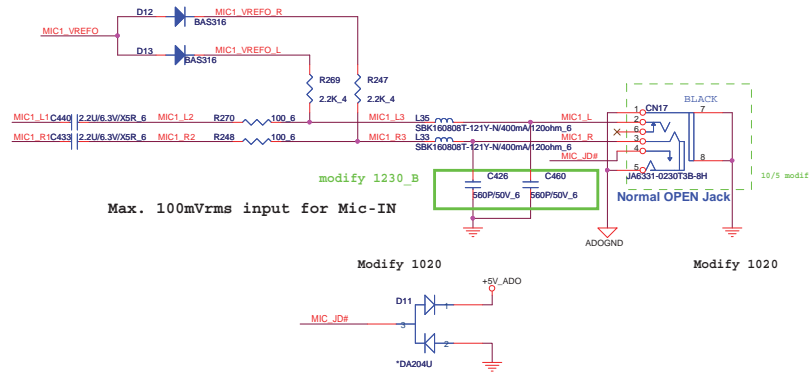
Headphone



INT. MIC



EXT. MIC



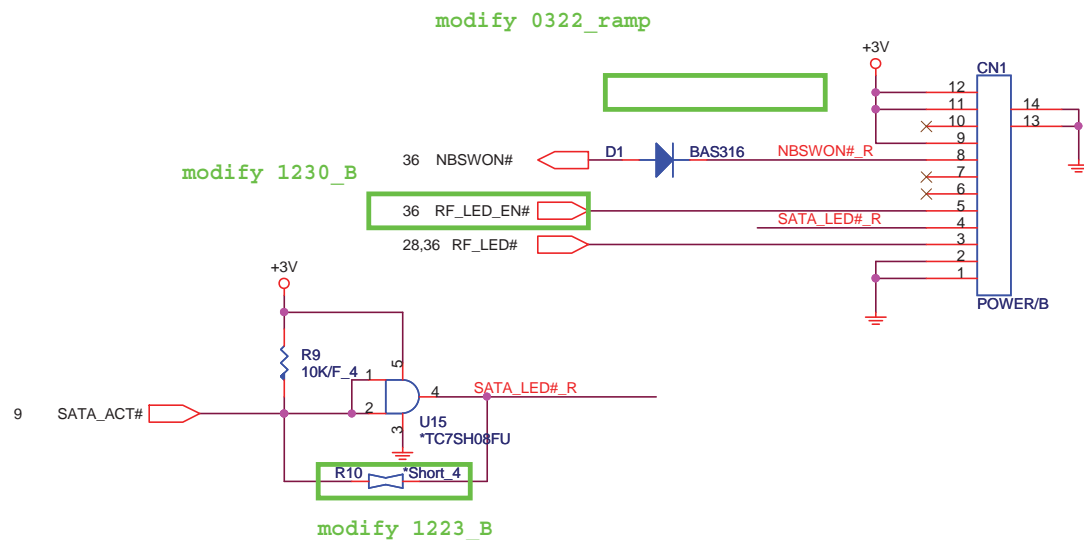


3

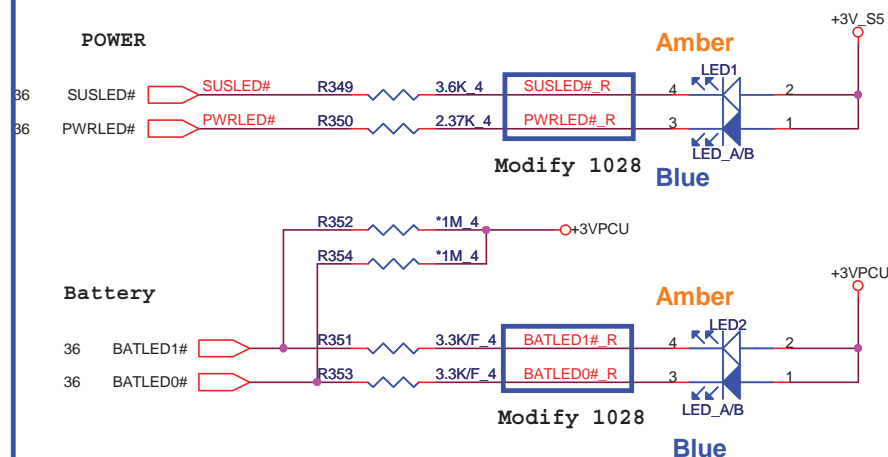
2

1

POWER BOARD CONN(UIF)



LED(UIF)

**Quanta Computer Inc.**

PROJECT : ZYD

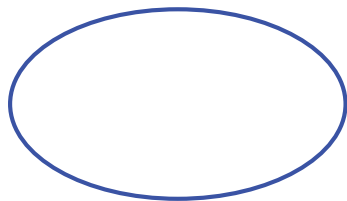
POWER/MMB/LAUNCH/LED

Rev
3B

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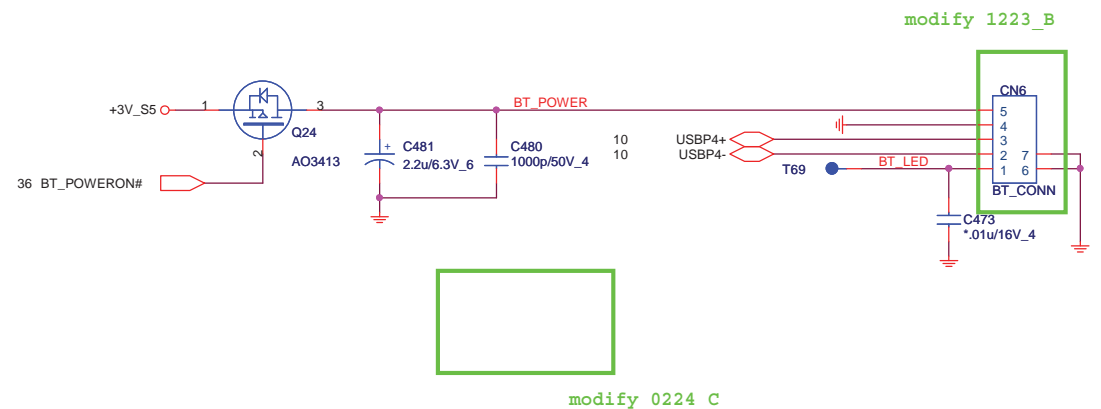
Date: Tuesday, April 06, 2010

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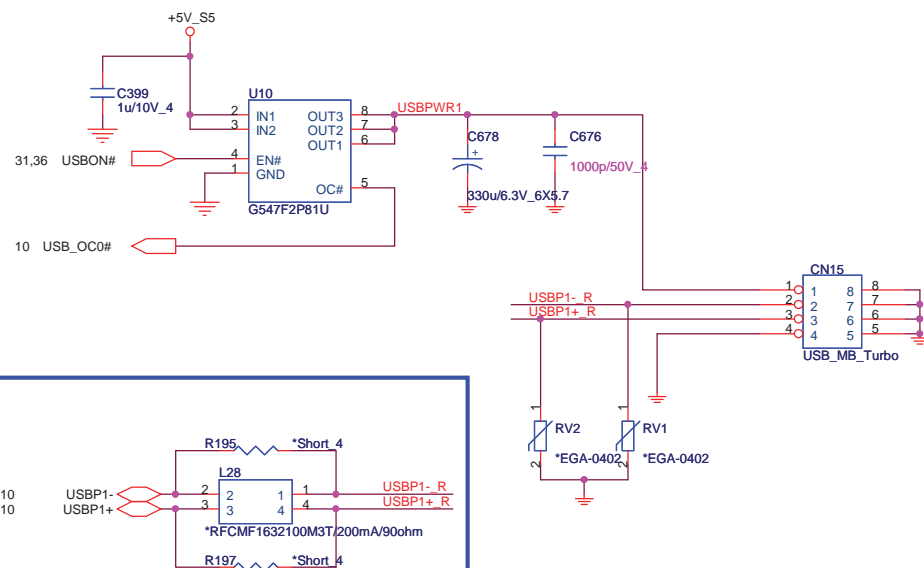


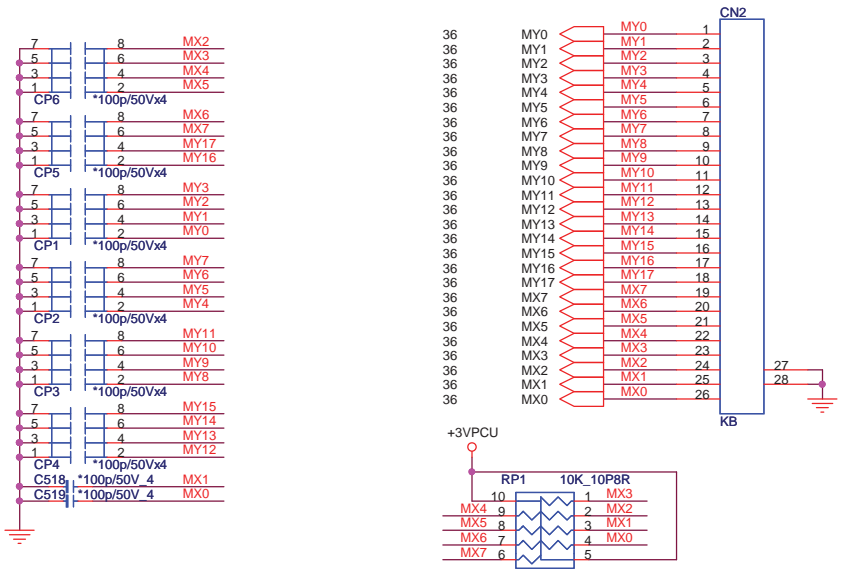
Modify 1022

BLUETOOTH CONNECTOR(BTM)

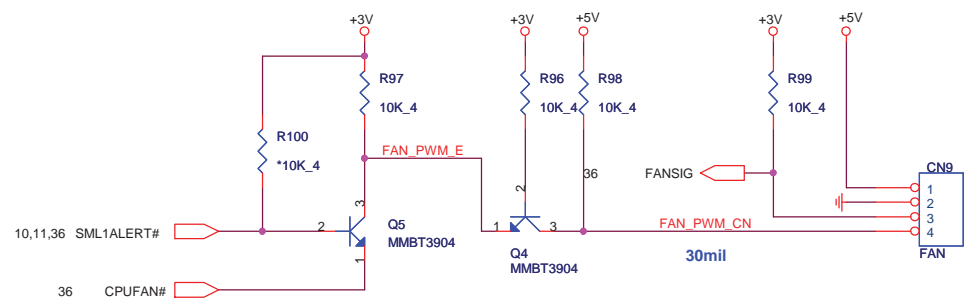


USBX1(USB)

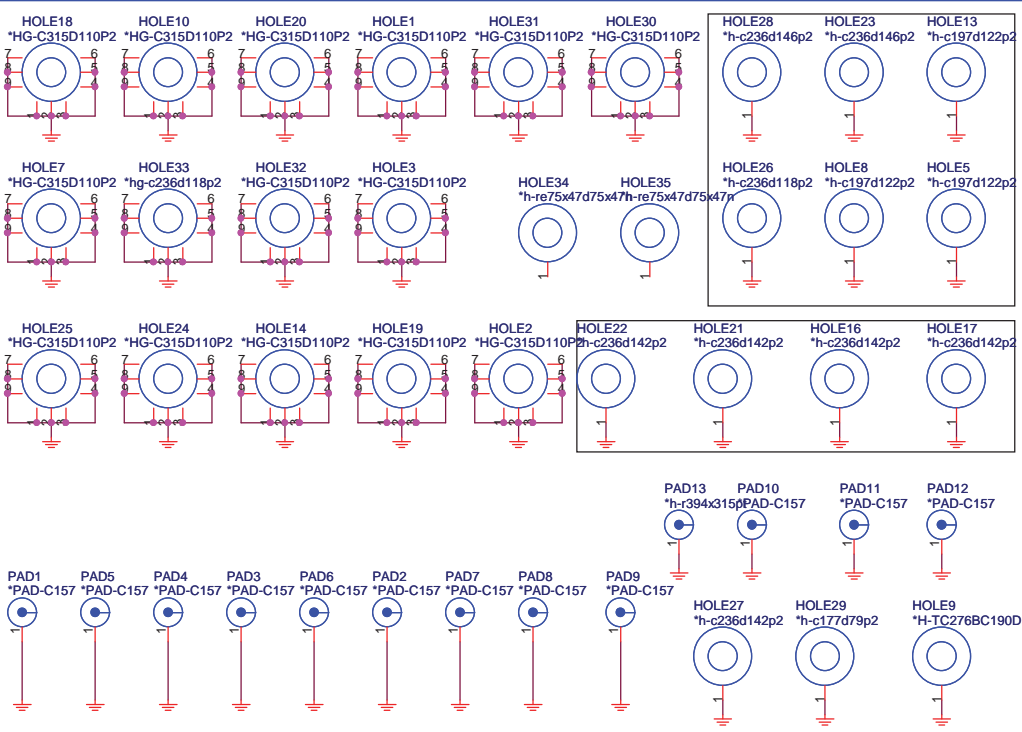
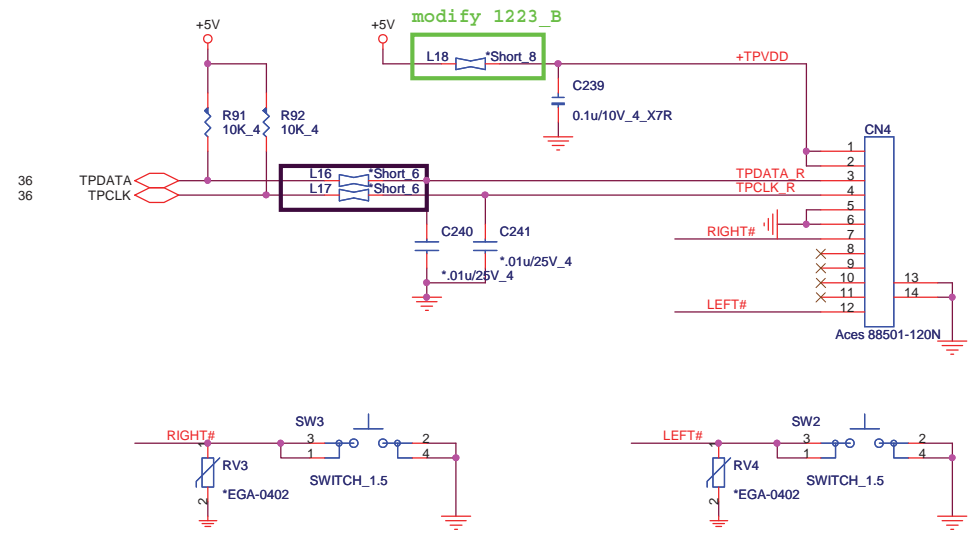





CPU FAN(THM)



TOUCHPAD & Switch CONN.(TPD)

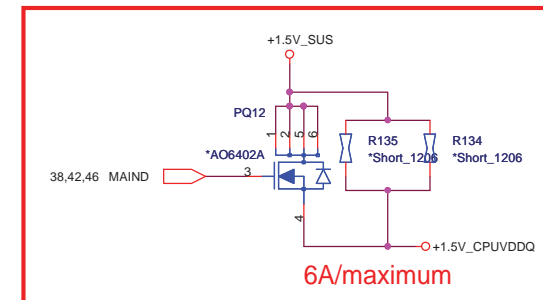
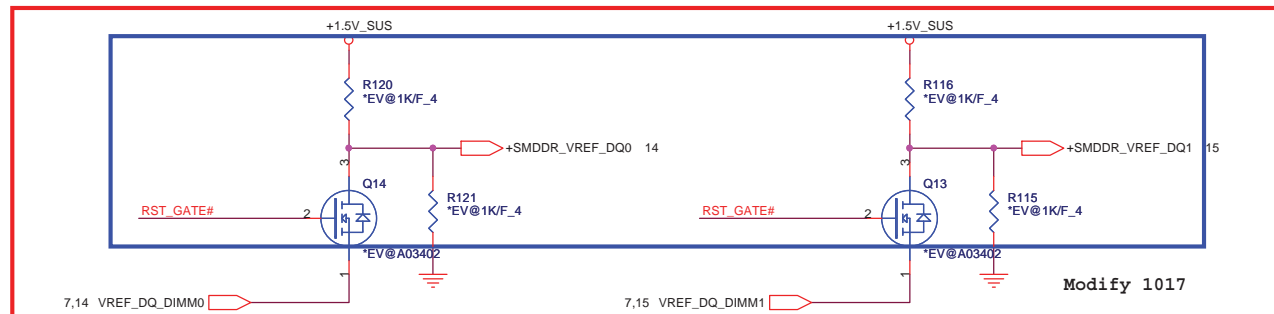
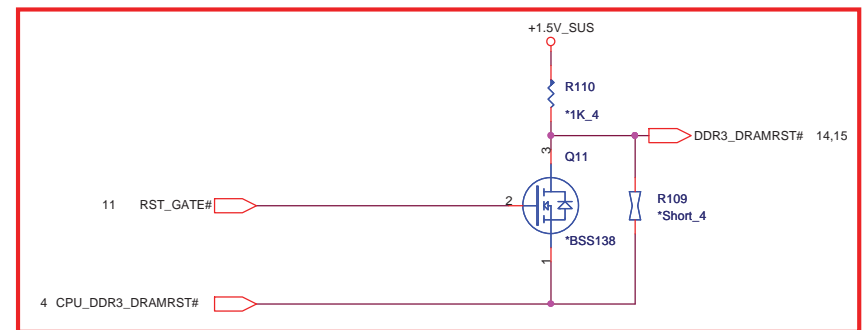
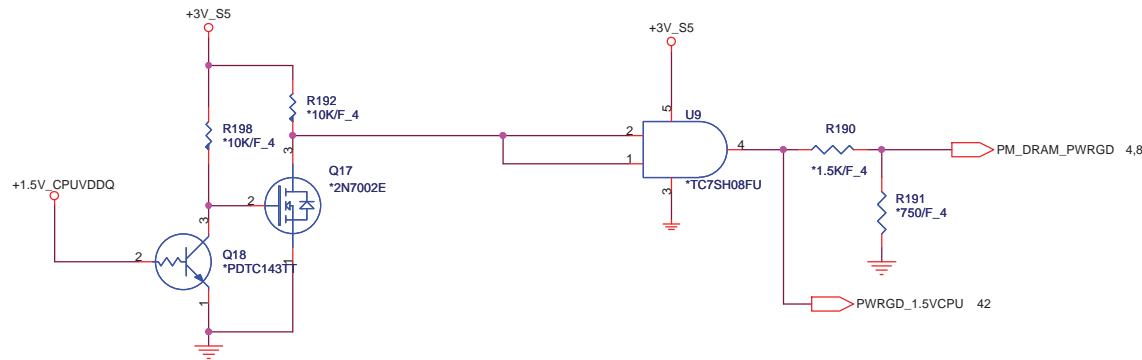
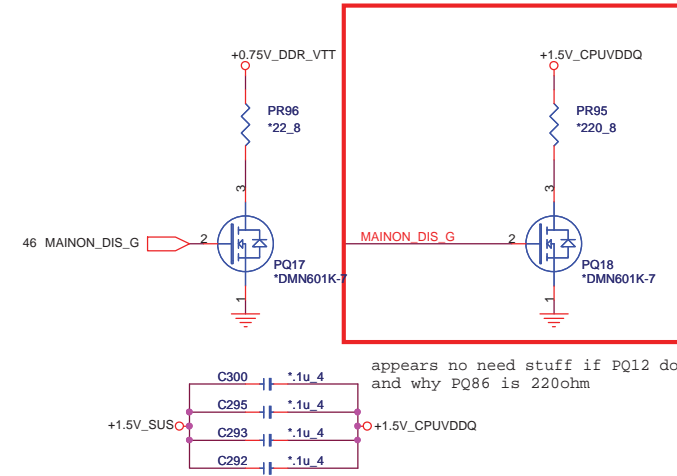




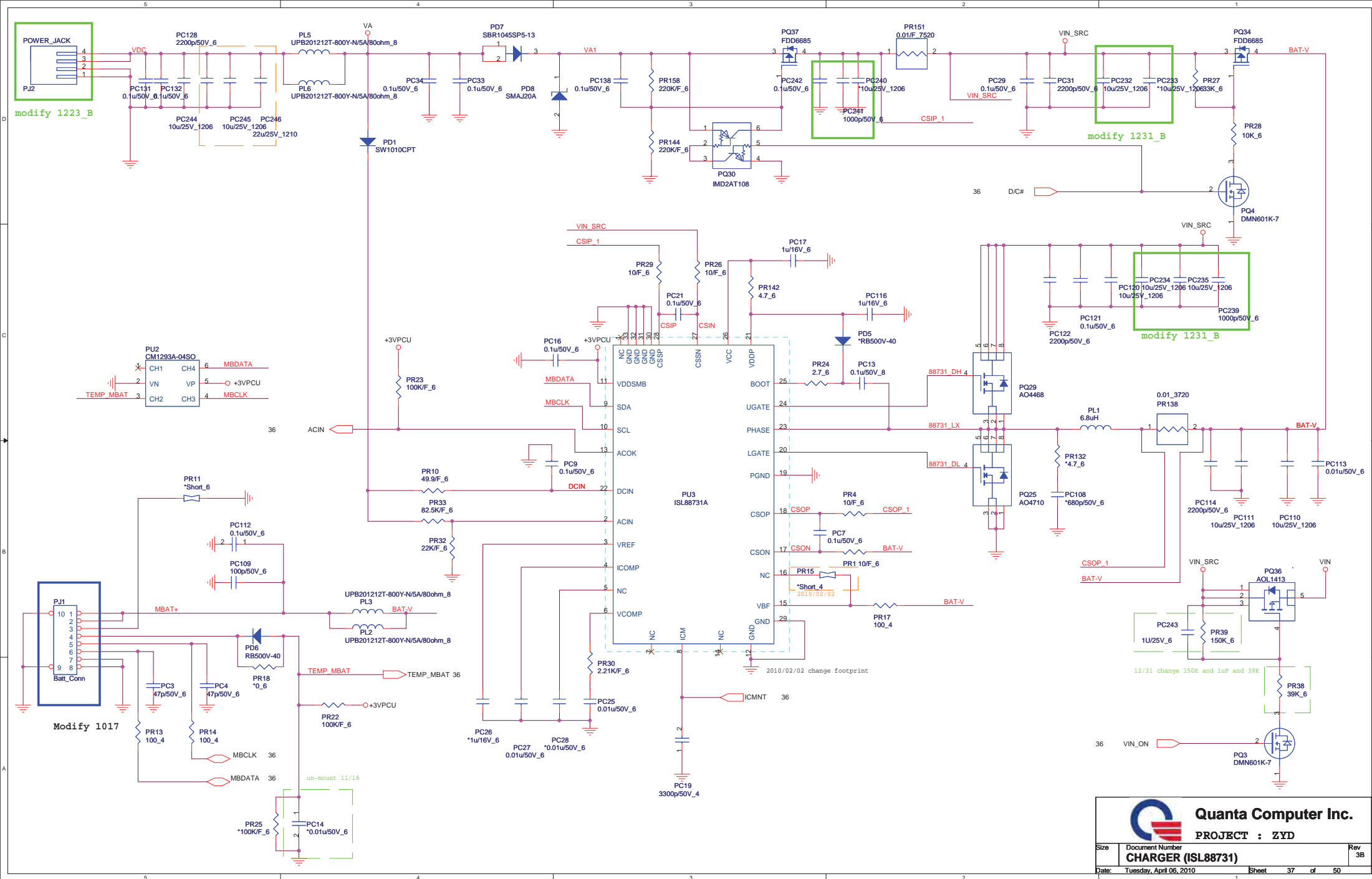
Quanta Computer Inc.
PROJECT : ZYD

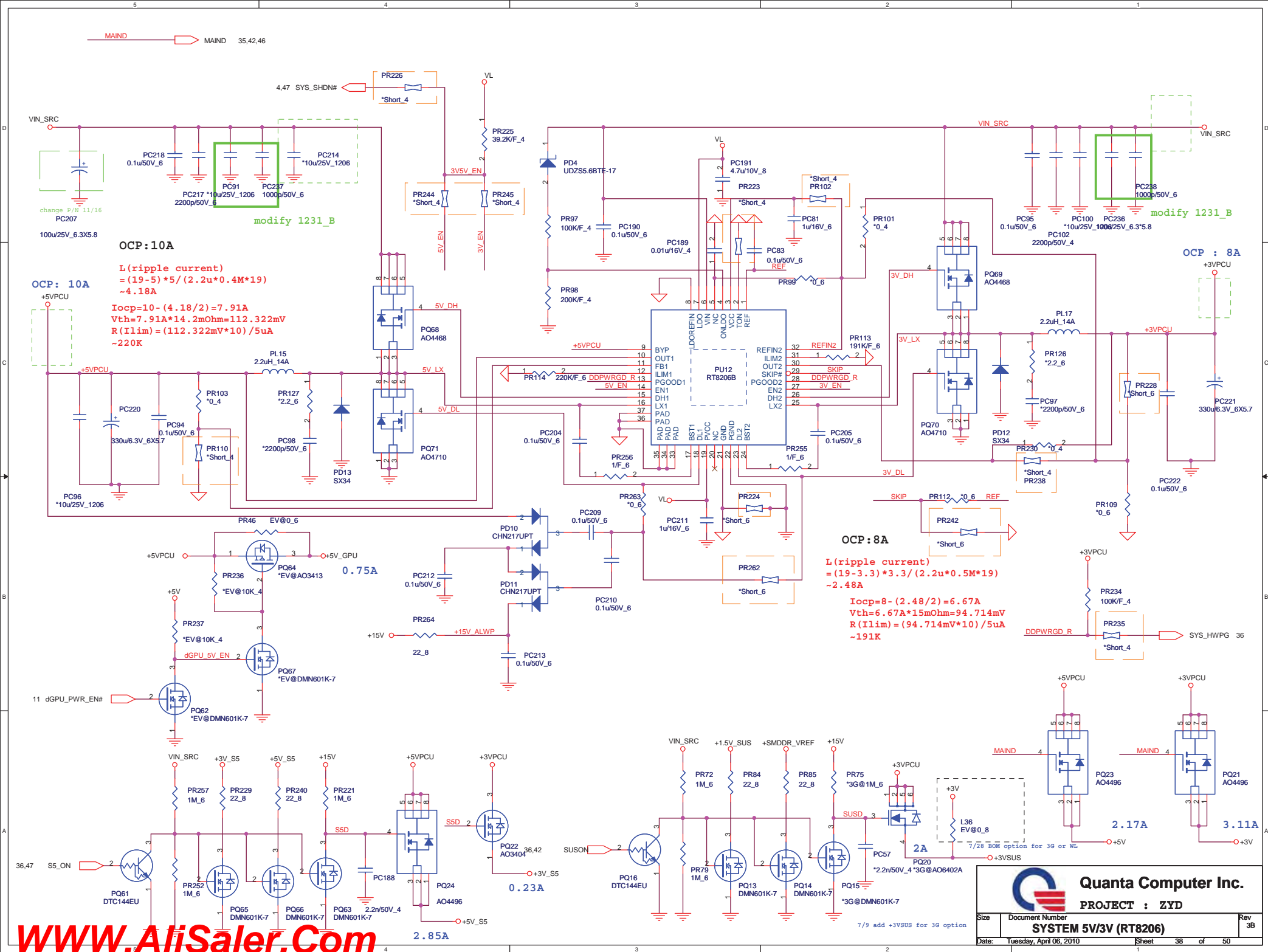
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SM_DRAMRST# signal (to system memory) to be driven high
 CKE signals (to system memory) to be driven low
 VREFDQ and VREFCA voltage (on system memory) needs to be maintained
 1.5-V power rail to system memory to be maintained.
 All other DDR3 memory interface signals are don't care during S3 state for
 memory self refresh.
 SM_DRAMPWROK (to processor) is driven low during S3 as Processor VDDQ (1.5 V)
 is turned off with this implementation.

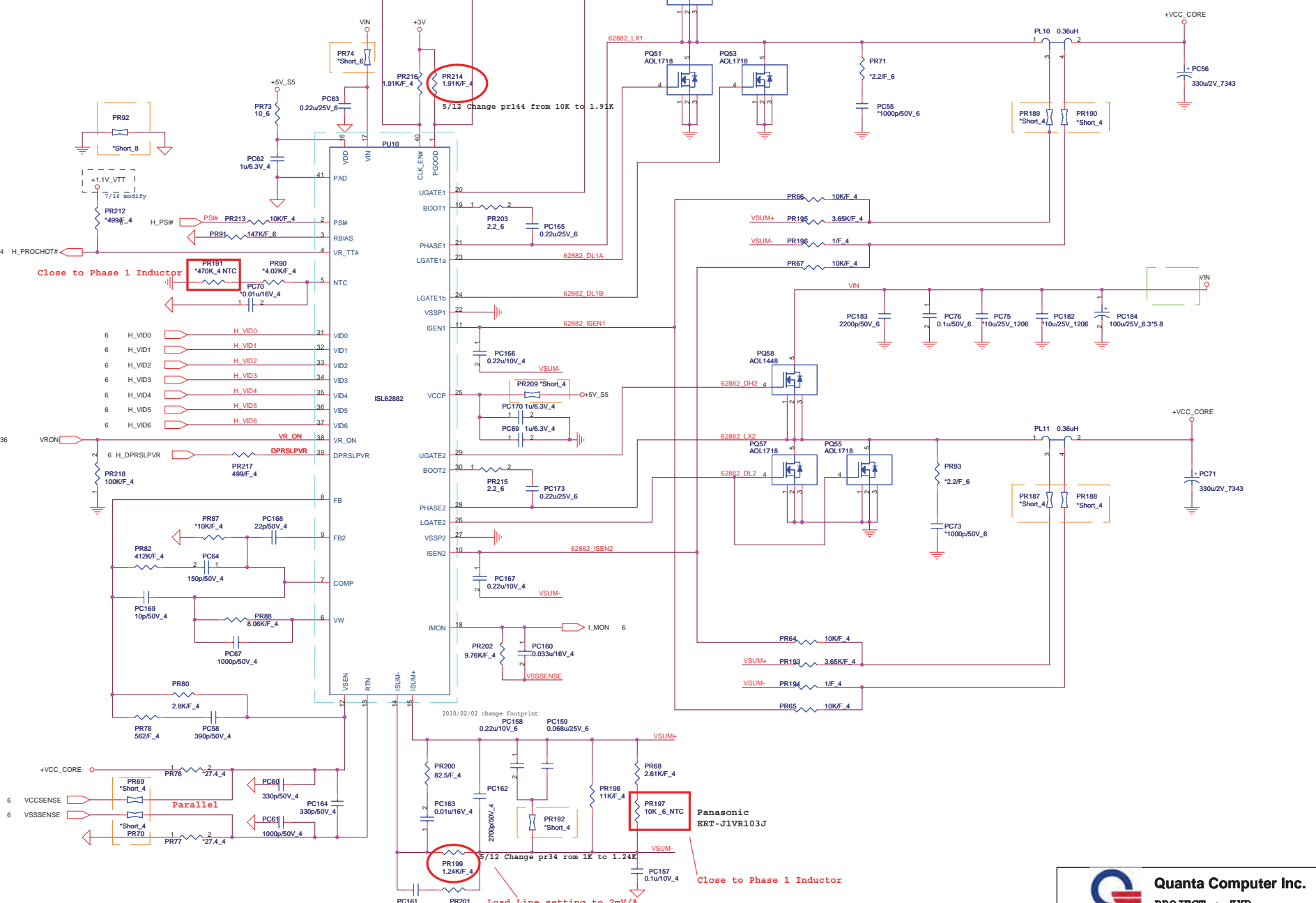


These isolation FETs are not required for ARD-only
 designs. Only CFD and common motherboard designs need to implement this circuit to
 meet the DDR3 VREF specification during S3.

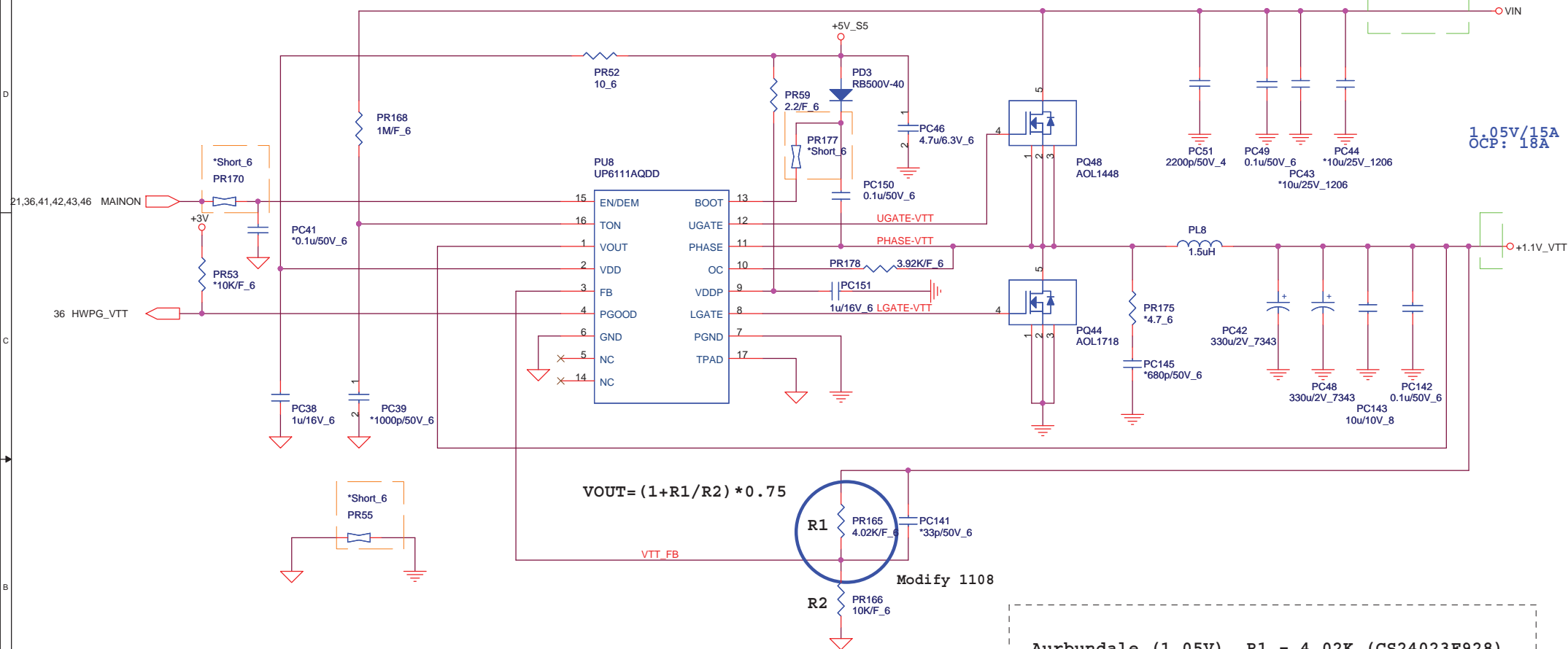




[PWM]



[PWM]



$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin * TON)$$

$$TON = 3.85p * 1M * 1 / (Vin - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$

AO1718 Rdson=3~4.3mOhm

$$L(ripple\ current) = (19 - 1.05) * 1.05 / (1u * 272k * 19) \sim 3.64A$$

$$4.3m * 18 = RILIM * 20uA$$

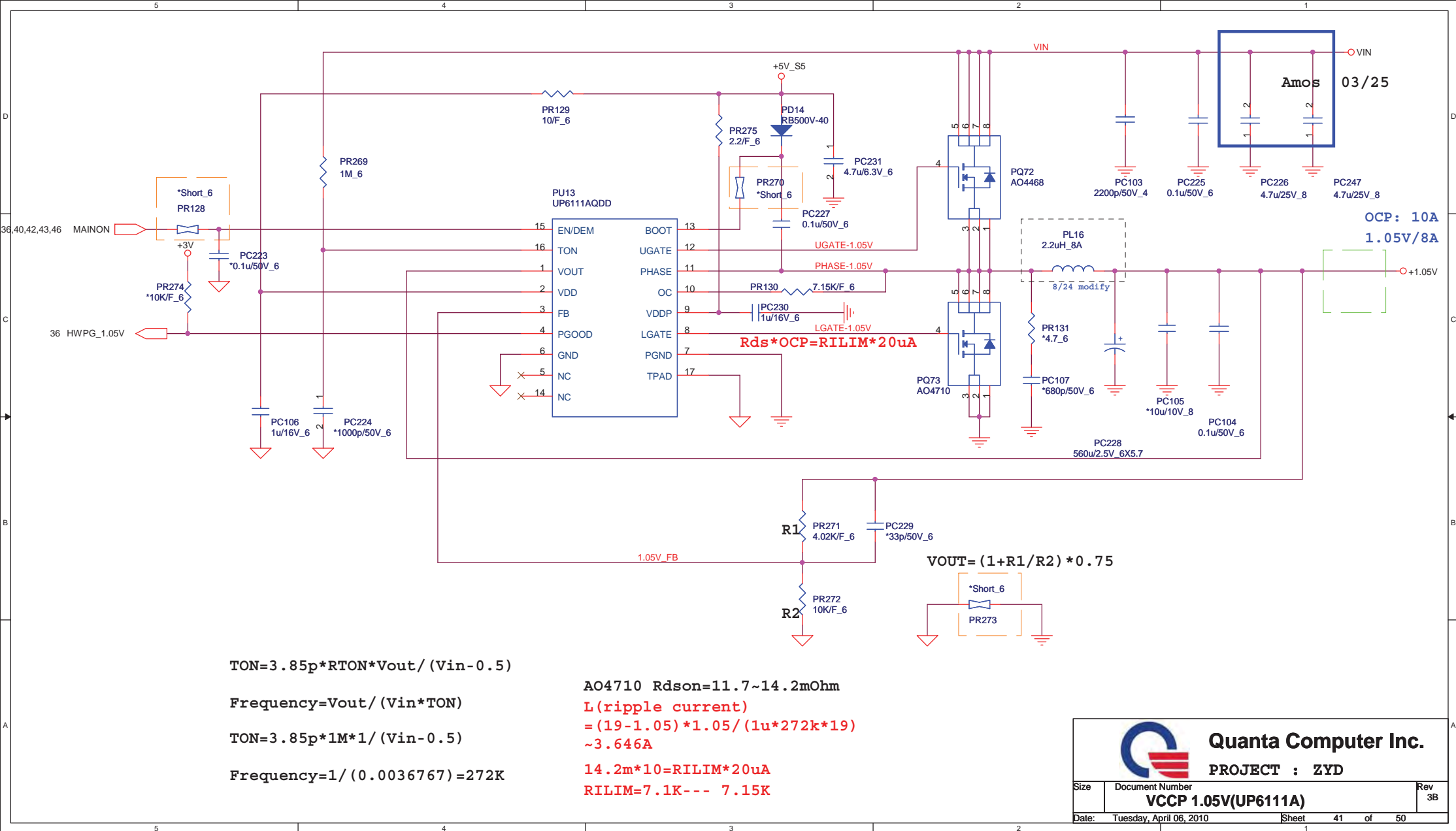
$$RILIM = 3.87K \text{ --- } 3.92K$$

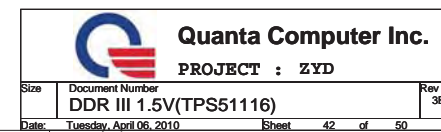
Aurbundale (1.05V) R1 = 4.02K (CS24023F928)
Clarksfield(1.1V) R1 = 4.75K (CS24753F919)

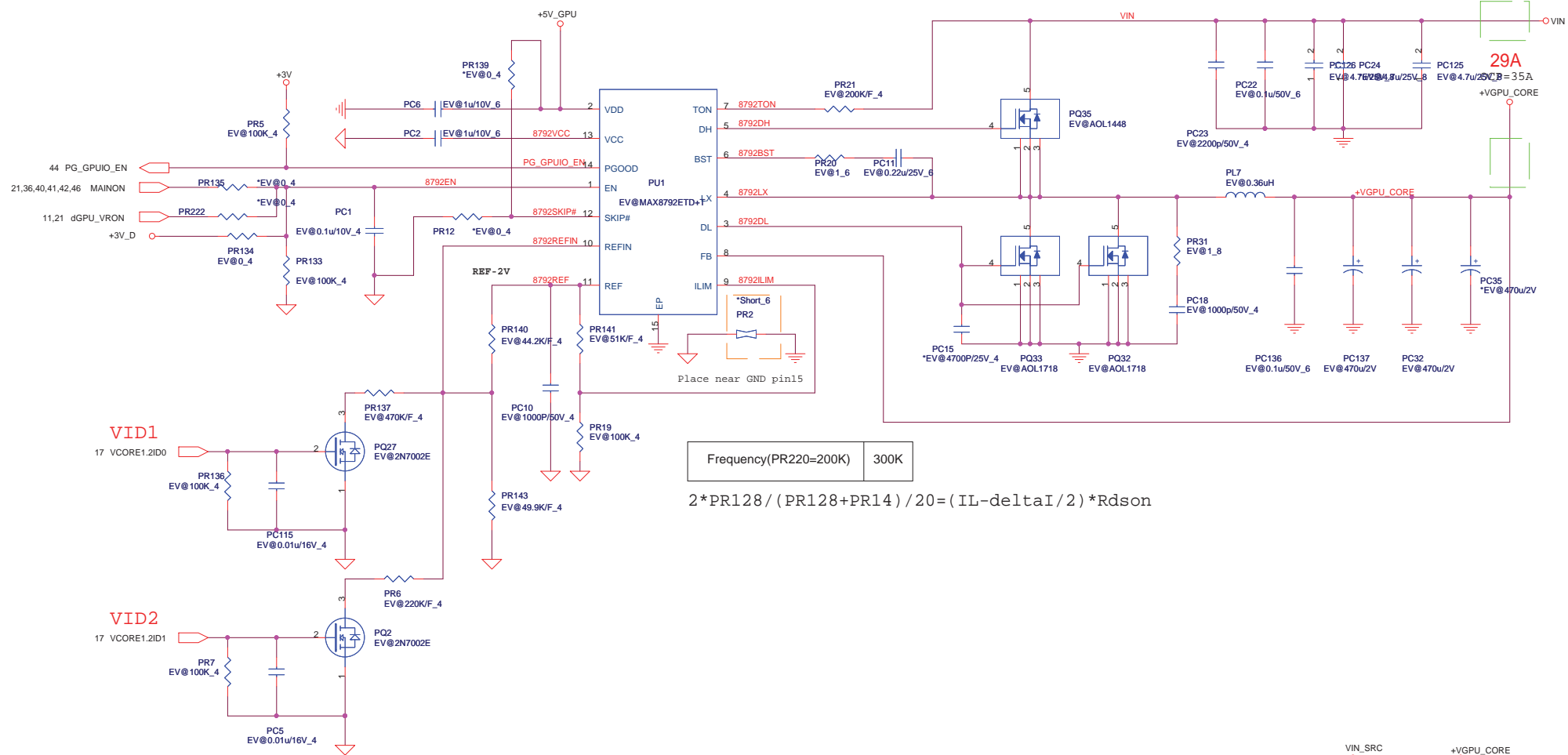


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Frequency(PR220=200K) 300K

$$2 * PR128 / (PR128 + PR14) / 20 = (IL - \Delta I / 2) * R_{dson}$$

Madison VID Table

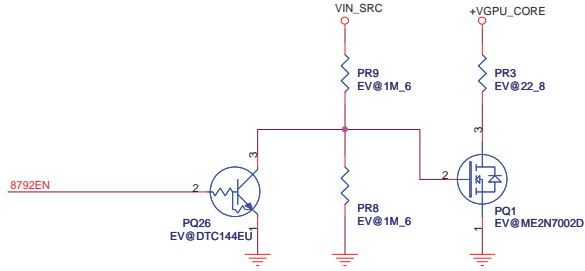
VID1		VID2			+VCC_GFX_CORE
VCORE1.2ID0	VCORE1.2ID1	VCORE1.2ID0	VCORE1.2ID1		
LOW (0)	LOW (0)			LOW (0)	1.05V
HIGH (1)	LOW (0)			HIGH (1)	1.0V
LOW (0)	HIGH (1)			LOW (0)	0.95V
HIGH (1)	HIGH (1)			HIGH (1)	0.90V

PR140 = 44.2K
PR143 = 49.9K
PR137 = 470K
PR6 = 220K

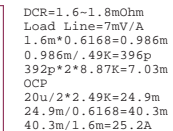
PARK XT VID Table

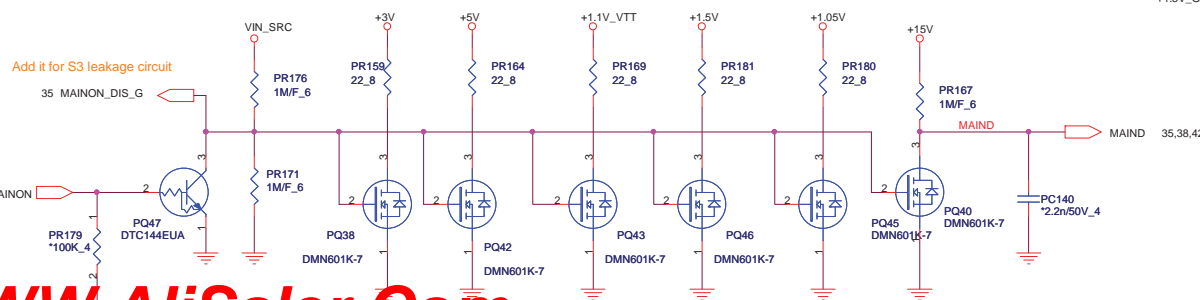
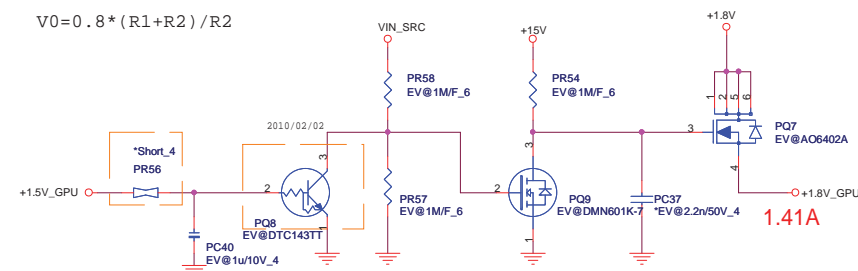
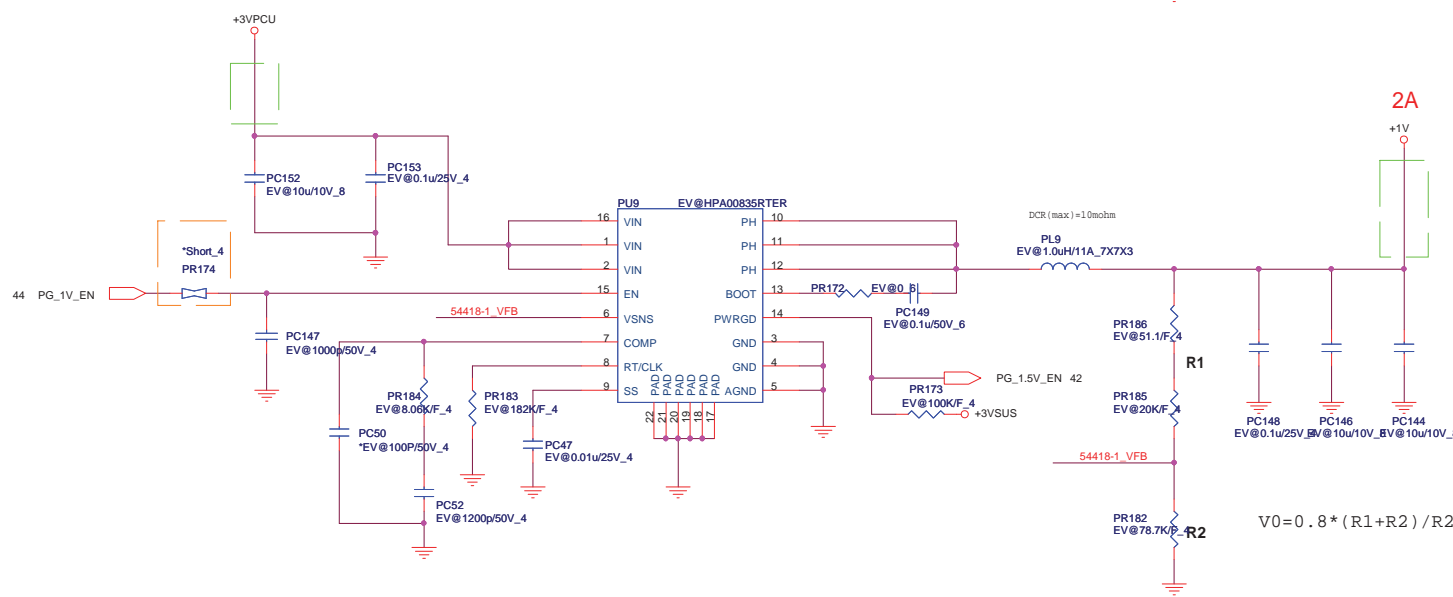
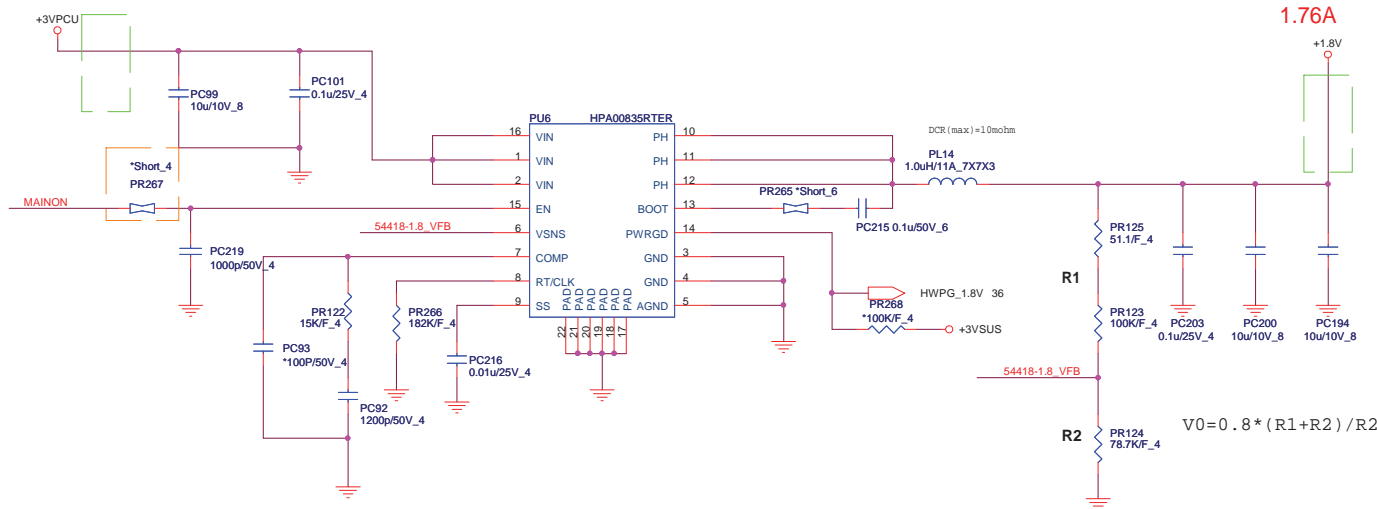
VID1		VID2			+VCC_GFX_CORE
VCORE1.2ID0	VCORE1.2ID1	VCORE1.2ID0	VCORE1.2ID1		
LOW (0)	LOW (0)			LOW (0)	1.12V
HIGH (1)	LOW (0)			HIGH (1)	1.05V
LOW (0)	HIGH (1)			LOW (0)	0.95V
HIGH (1)	HIGH (1)			HIGH (1)	0.90V

PR140 = 39.2K CS33922FB15
PR143 = 49.9K CS43322FB15
PR137 = 332K CS41302FB00
PR6 = 130K

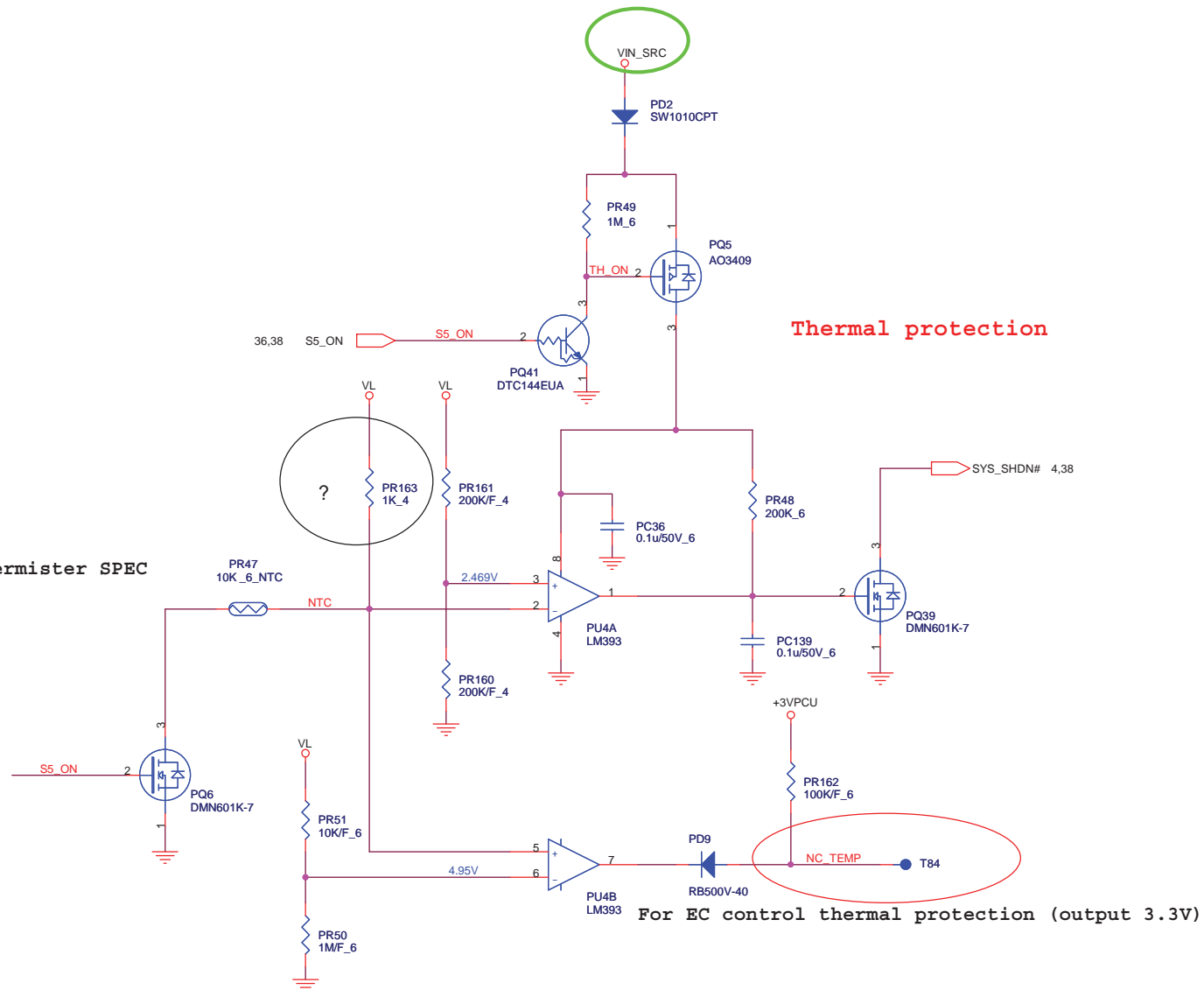








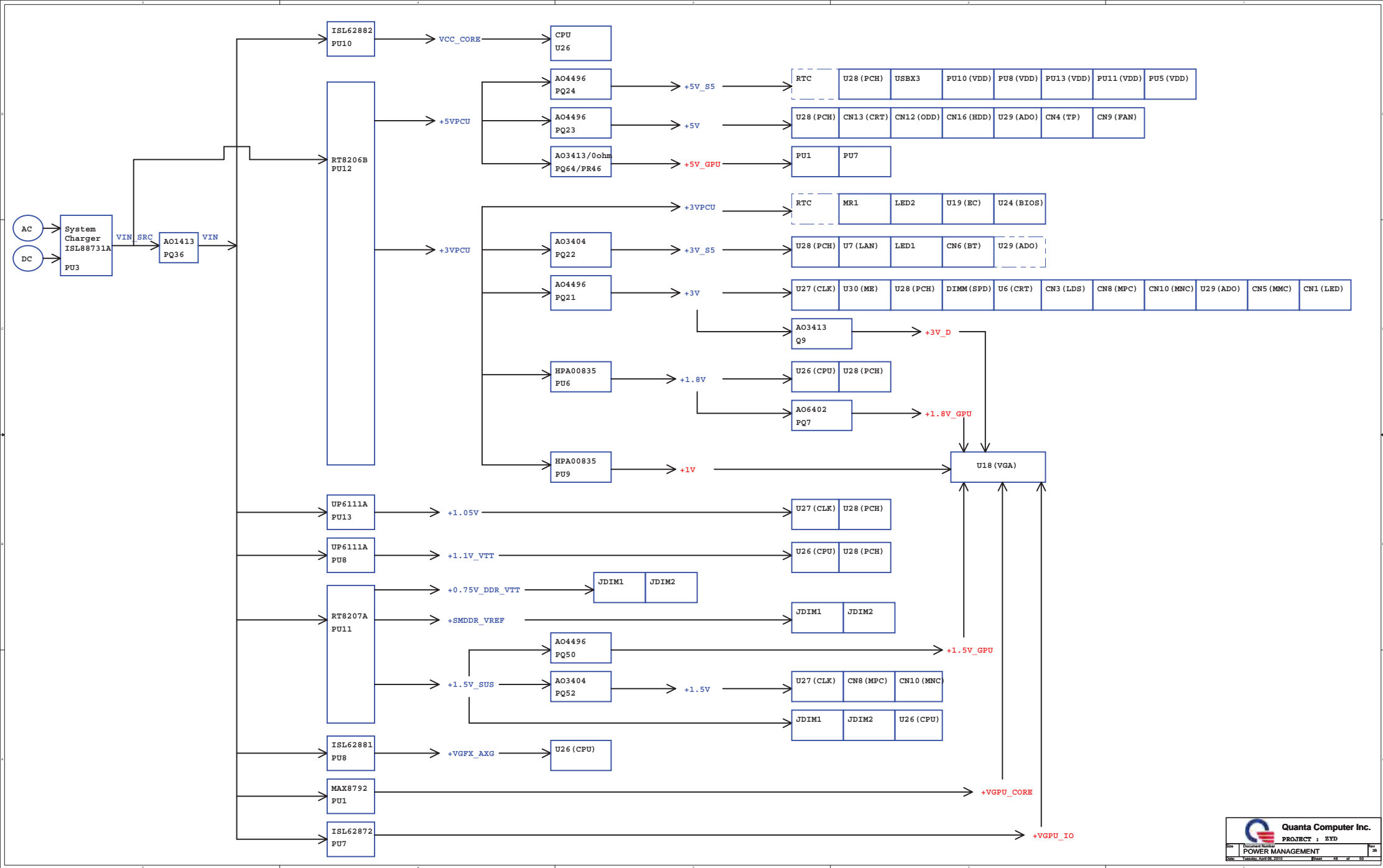
based on thermister SPEC
1K--->82~83



Quanta Computer Inc.

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Model	REV	CHANGE LIST	MODEL	ZYD		
				FROM	To	
ZYD MB	1A	20091028 Page 30, Move the resistors and common chokes from M/B to daughter board	X	1A		
		20091028 Page 30, Move the R1027 and R1059 to daughter board and change to 0402 (place closer).	X	1A		
		20091028 Page 30, Move USB Power switch to daughter board	X	1A		
		20091028 Page 30, Change card readersUSB board CONN P/N to DPFC20PR255	X	1A		
		20091028 Page 26, Delete R203 and R171 to leave RJ45 chasias contact to GND directly	X	1A		
		20091028 Page 31, Add net name sused#_R, Pwled#_R,BATLED0#_R, BATLED1#_R,RFLED#_R,RFLLED2#_R	X	1A		
		20091028 Page 35, Add SW1 for debug purpose	X	1A		
		20091028 Page 33, update Hole footprints	X	1A		
		20091029 Page 41, Change PR199, PR200 P/N from CS000003J951 to CS000003P916	X	1A		
		20091102 Page 24, 29, Add Mic_GND for internal analog MIC	X	1A		
20091102 Page 27, Delete C204, C208, C558, R411, R385, R373, RP3, Q27, Q26. and change C578 from 0.47u to 4.7u	X	1A				
20091102 Page 10, Stuff R1001, R1002, R503	X	1A				
20091103 Page 33, Delete Hole4, Hole5, Hole8, Hole18	X	1A				
20091104 Page 33, update power schematic	X	1A				
20091104 Page 30, swap L38,L39,L58 USB nets for layout request.	X	1A				
20091108 Page 45, delete net name MAIN0W_0	X	1A				
20091108 Page 39, Change PR151 P/N from CS24703P908 to CS24023P928 for support Arrandale only	X	1A				
20091108 Page 33, Delete Hole36	X	1A				
20091110 Page 31, Move Wi-Fi LED to PB	X	1A				
20091111 Page 39, Delete P18 and Change P18 footprint and value(1.5uH footprint:CHOKE-ETQP4LR36WPC-NB4)	X	1A				
20091111 Page 41, Stuff +1.5V_GPU power source for EVB only	X	1A				
20091111 Page 37, reserve PR275 for GPU power	X	1A				
20091112 Page 18, Follow ATI suggestion to modify R419 from 680ohm to 51 ohm.	X	1A				
20091112 Page 27, Remove LPC from Mini PCIE port CN24	X	1A				
20091112 Page 37,45, unstuff +3V_SUS components	X	1A				
20091113 Page 27, Two Wi-Fi LED share one net RF_LED#	X	1A				
20091113 Page 31, Delete Q21,Q23, R347	X	1A				
20091113 Page 29, Reserve three more resistors R373, R368, R385 for ESD solution	X	1A				
20091116 Page 34, unstuff PR95, PR96, PQ17, PQ15	X	1A				
20091116 Page 24, Change C650 from 0.22u/6.3V_4 to 0.22u/10V_4	X	1A				
20091116 Page 32, Change C399 from 1u/6.3V_4 to 1u/10V_4	X	1A				
20091116 Page 7, unstuff R159	X	1A				
20091116 Page 11, stuff R592 for DIS and stuff R595 for UMA	X	1A				
20091116 Page 11, Reserve pull low for unused pin dGPU_VMON_R	X	1A				
20091116 Page 8, Delete R414	X	1A				
20091116 Page 25, Delete R162	X	1A				
20091116 Page 36-45, PC14 un-mount/ PC207 change P/N/ PC154 change P/N and value./ PC155 un-mount/ PC180 change P/N/ PC119 change P/N/ PC118 change P/N	X	1A				
2A		20091119 Page 36, Modify Bat CONN P/N and footprint	1A	2A		
		20091119 Page 29, Modify Speaker CN7 P/N from DFHD04MR779 to DFHD04MR057	1A	2A		
		20091120 Page 8`13, Modify PCH P/N from A30QMS0T05 to A3SLG2S0T07	1A	2A		
		20091124 Page 27, Short Pin42 and Pin44 of CN8 and CN10 to support Intel WIMAX/WiFi combo module	1A	2A		
		20091128 Page 37, stuff L36 for discrete sku	1A	2A		
		20091128 Page 9, change U30(MR ROM) P/N from AKE391P0M00 to AKE38ZP0M01	1A	2A		
		20091202 Page 3, reserve 1U for CLK GEN +1.5V power	1A	2A		
		20091203 Page 27, Stuff Q26 and Q28; unstuff R401 and R447; and add LPC bus to CN24 for debug purpose	1A	2A		
		20091209 Page 42, add VID table for Park XT	1A	2A		
		20091209 Page 3, change R257 from 0ohm to 33ohm	1A	2A		
		20091209 Page 3,17,18 follow AMD suggestion to stuff R257, R101, R407,R409 and remove R36 to fix AMD pre-production silicon bug	1A	2A		
		20091214 Page 9, change R317 to a JP and stuff R322	1A	2A		
		20091214 Page 32, change CN6 from DFHD05MRD98 to DFWF05MR027	1A	2A		
		20091221 Page 29, change R533 from CS03923P916 to CS33922P915	1A	2A		
		20091223 Page 10, change R202, R203, R540, R566, R547 to short pad	1A	2A		
		20091223 Page 36, change DC jack P/N to DFH804FR741	1A	2A		
		20091223 Page 32, change CN6 P/N to DFWF05MR012	1A	2A		
		20091225 Page 50, change CN19 P/N to DFHD19MR083	1A	2A		
		20091230 Page 12, Add C786 for CRT flicker issue	1A	2A		
		20091230 Page 27, change transformer footprint to TRF-10-1-24P-SMT	1A	2A		
		20091230 Page 17, change VGPU_CORE VID control pin	1A	2A		
		20091230 Page 28, Exchange P/N for cn8 and cn10	1A	2A		
		20091230 Page 28, Move controller link from CN10 to CN8	1A	2A		
		3A		20100129 Page 32, remove power LED MOS Q25	2A	3A
				20100130 Page 18, Remove AMD option 2 workaround for Madison and Park; and change R36 from 1K to 10K	2A	3A
				20100130 Page 28, Change Mini card footprint to MIPCI-800055F80520X-52P-LDV-NB4	2A	3A
				20100201 Page 32, restore power LED MOS Q25	2A	3A
				20100201 Page 25, Change Q33,Q34 to ESD protection part	2A	3A
20100222 Page 24, Reserve C787 and C788 for CRT flicker issue	2A			3A		
20100222 Page 36, Remove SW1	2A			3A		
20100222 Page 12, Add C789 for VCCADAC	2A			3A		
20100222 Page 17, Reserve 10U*2 caps for +1.5V_GPU	2A			3A		
20100222 Page 30, Add short Pad R635,R636,R637,R638,R640 for RMI	2A			3A		
20100222 Page 24, unstuff L13 and stuff R89 and R90	2A			3A		

[illegible]